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14. ABSTRACT

This research focuses on a kW-level active-bridge DC-DC converter. Using two hardware prototypes, the study contraste the performance of the inverter-bridge section of the converter using either state-of-the-art Silicon (Si) or Silicon Carbide (SiC) MOSFETs. Innovations in SiC MOSFET technology have facilitated reductions in steady-state switch losses and operation at higher device temperatures. By enabling reductions in losses and higher-temperature operation, converter thermal management requirement is decreased. Thus, SiC devices offer the possibility of increased converter power density. Converter power density is evaluated by measuring the maximum power throughput of the converter for a given maximum device junction temperature. The physical volumes of the two converters are held fixed so that throughput power will represent a means of directly quantifying power density. In this paper, the design of the converter is detailed, including gate drivers and snubber circuitry, and testing results are presented.

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AN INVESTIGATION OF DC-DC CONVERTER POWER DENSITY USING Si AND SiC MOSFETS

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Abstract

As the U.S. Navy moves forward in developing Next Generation Integrated Power Systems (NGIPS) for future surface combatants, constraints on space and weight require a continued increase in converter power density. Further, with the Navy‟s interest in medium-voltage DC (MVDC) architectures, DC-DC converters will play a prominent role interfacing the medium-voltage bus with the lower-voltage distribution system and energy storage resources. This research focuses on a kW-level active-bridge DC-DC converter topology as it offers magnetic isolation, a requirement of the SSCM design for a MVDC system. Using two hardware prototypes, this study will contrast the performance of the inverter-bridge section of the converter using either state-of-the-art Silicon (Si) or Silicon Carbide (SiC) MOSFETs. Innovations in SiC MOSFET technology have facilitated reductions in steady-state switch losses and operation at higher device temperatures. By enabling reductions in losses and higher-temperature operation, converter thermal management requirement is decreased. Thus, SiC devices offer the possibility of increased converter power density.

For this investigation, converter power density is evaluated by measuring the maximum power throughput of the converter for a given maximum device junction temperature. Si and SiC devices are processed so that a thermal imaging system can conveniently monitor the steady-state device temperatures. In the design process, the physical volumes of the two converters are held fixed so that throughput power will represent a means of directly quantifying power density. In this paper, the design of the converter is detailed, including gate drivers and snubber circuitry, and testing results are presented. Specifically, it was found that SiC devices produced a 188.3 percent improvement in maximum power throughput and power density. Using SiC, desired Navy power density figures for the MVDC architecture can be fulfilled and implemented in volumetrically constrained shipboard environments.

Acknowledgements

I would like to thank Professor Ciezki and Professor Salem for their unwavering guidance and support through this project. I would also like to thank the Electrical Engineering Laboratory Technicians, specifically Ken Walsh, Bill Stanton, Bonnie Jarrell, Eric Keyes, ET2 Dante Marasco, and Daphi Jobe. They have always been able to provide a smiling face, a joke and excellent technical assistance with any problem I might have had over the year. I would finally like to thank the Trident Committee and Professor Wick for their assistance and efforts.

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List of Symbols Used

B_{Max}, Maximum Magnetic Flux Density in an Inductor
$C_{DS,}$ MOSFET Drain to Source Capacitance
C_{GD}, MOSFET Gate to Drain Capacitance
C_{GS}, MOSFET Gate to Source Capacitance
D, Duty Cycle
E_G, Semiconductor Bandgap Energy
$f_{sw,}$ Converter Switching Frequency
i_{pk}, Peak Primary Current Level
$i_{rect,out,ave}$, Rectified Average Output Current
k_B, Boltzmann‟s Constant
K_{fe}, Frequency Dependent Loss Constant
L_L, Leakage Inductance
$N,$ Transformers Turns Ratio
P_{Loss}, Semiconductor Power Losses
$R_{DS,on}$, MOSFET On State Resistance
R_{OUT}, Output Load Resistance
$T_{J,MAX}$, Maximum Junction Temperature
β, Loss Exponent Factor
ΔB_{opt}, Optimal Flux Density Swing in Transformer
η_{SYS}, System Efficiency
λ_1, Transformer Primary Flux Linkage
$\rho_{conv,}$ Power Density

List of Abbreviations

ABM – Anti Ballistic Missile
AC – Alternating Current
ARL – Army Research Laboratory
DC – Direct Current
DCM – Discontinuous Mode
HFAC – High Frequency AC
IGBT – Insulated Gate Bipolar Transistor
IPS – Integrated Power System
MOSFET – Metal Oxide Semiconductor Field Effect Transistor
MVAC – Medium Voltage AC
MVDC – Medium Voltage DC
NGIPS – Next Generation Integrated Power System
ONR – Office of Naval Research
PCM-1A – Power Conversion Module, 1A
PGM – Power Generation Module
RMS – Root-mean-square
SAB – Single Active Bridge Topology
Si – Silicon
SiC – Silicon Carbide
SSCM – Ships Service Converter Module

I. Introduction

Currently, the Navy is investigating the use of an Integrated Power System (IPS) as the primary power distribution architecture for future naval combatants. In an IPS, all mechanically-derived power generated aboard ship is converted to electrical form, which is then distributed to loads ranging from propulsion to high energy weaponry. This system differs from the power generating capability in current naval vessels in that modern power distribution systems have the majority of mechanical power generated chained through reduction gears to propulsion, and not available for other uses. IPS architectures offer the ability to handle high energy electrical loads and propulsion simultaneously.

As energy demands of shipboard loads increase, shipboard power generating capability must increase as well. This growth in demand upon the shipboard power generation system is shown in Figure 1. [7] The currently designed IPS architecture in the DDG-1000 class destroyer can accommodate all electrical loads while driving propulsion at flank speed. However, with the advent of higher energy weapons loads, such as high power anti-ballistic missile (ABM) radar, pulsed-power weapons, railguns and high energy free-electron laser weaponry, power demand will quickly outstrip generating capability. Either additional generating capability must be installed or novel control, energy storage, and power distribution capabilities must be implemented.

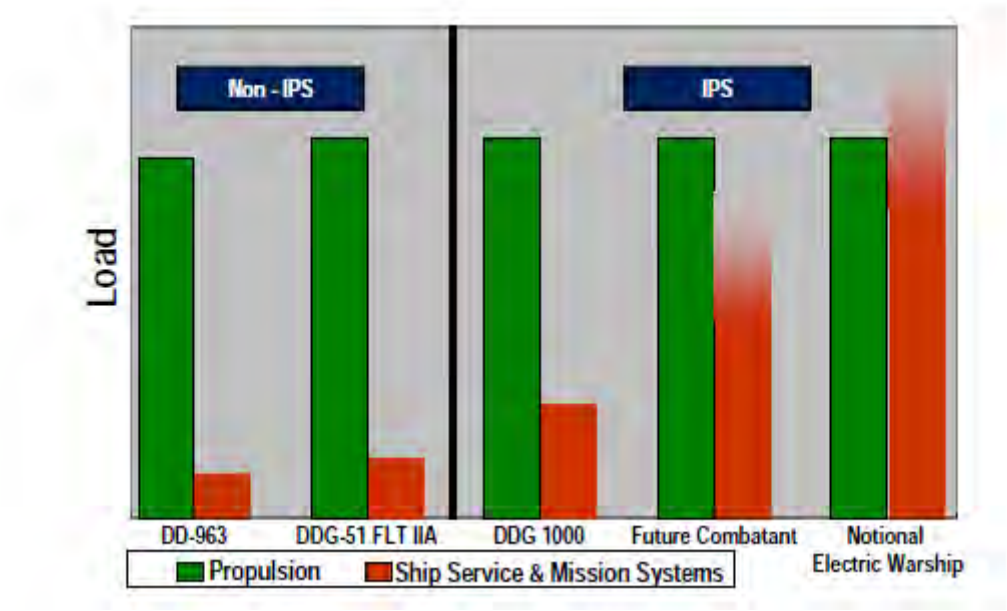

Figure 1 - Power Demands of Present and Future Naval Combatants [7]

In order to accommodate the increased power demands of future shipboard loads, dedicated high power generators have been proposed to power each load individually. [7] However, increasing dedicated shipboard power generating capability quickly becomes prohibitive due to shipboard weight and volume constraints. In a platform such as a submarine or small surface combatant, volumetric constraints quickly become extremely prohibitive. Dedicating generators for high power loads takes up vital mission space and decreases functionality. Further, prime movers used for generation cannot respond to the instantaneous demands in power required by newer pulsed power weaponry and radar systems. It is necessary to use novel distributed energy generating capabilities, and energy storage banks to overcome this constraint. In an IPS architecture, energy can be directed to charge energy storage devices for high energy loads, and can also be redirected for use throughout the system. The ability to direct excess energy to storage devices effectively overcomes the volumetric constraints associated with increasing power demands in future electric ship combatants.

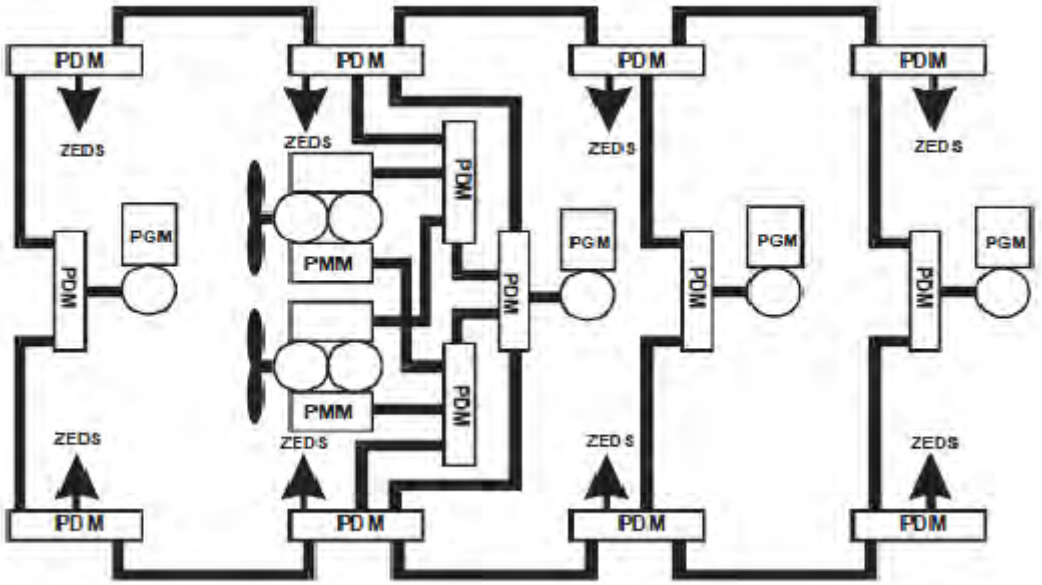

Figure 2 - Notional IPS Architecture [7]

Various IPS distribution topologies have been proposed for use within shipboard distribution systems. The notional architecture of an overall IPS distribution network is shown in Figure 2. A power generation module (PGM), taking the form of a mechanical engine, drives a generator to produce an electrical voltage. This voltage is changed according to the requirements of the distribution topology. A major limiting factor within each topology is the volume of the voltage manipulation elements. Currently, the first IPS architecture, designed to use medium voltage AC (MVAC) voltages, is being developed for the DDG 1000 and is also planned to be used in large surface combatants where significant volumetric constraints are not present. Though functionally capable, this topology has distinct disadvantages. Transformers employed within power distribution modules (PDMs) in the MVAC scheme are large and heavy. They are impractical for energy storage applications without additional power conditioners, and cannot be paralleled effectively for higher power loads. A solution is proposed in the form of a second topology, which uses higher frequency AC (HFAC) voltages. HFAC

alleviates some of these problems by raising the frequency of the distribution bus voltage to the 240 Hz to 400 Hz level, decreasing transformer size. However, the HFAC scheme still does not address directed energy storage.

The third and final considered IPS topology makes use of medium voltage DC (MVDC) voltages in the PDMs that interface to the distribution bus. This topology is optimal for volumetrically constrained environments, as it eliminates prohibitively large and heavy transformers. Instead, power is conditioned by power electronic modules that adjust voltages to necessary levels for multiple applications. Energy storage elements can be effectively integrated into an MVDC scheme. Though transformers are eliminated within this scheme, it is still necessary that the power electronic converters become significantly more power dense to offer improvements over previously discussed distribution topologies. Individual converter power density is a complex issue that must be investigated thoroughly to optimize the overall power density of the MVDC system.

II. Background

To understand the methodology through which power electronic converters are optimized, it is necessary to understand the principles through which power density may be maximized within a power converter. To accomplish this, an understanding of the general principle of DC-DC voltage conversion will be introduced. The distribution of volume within a practical converter, and effects of the converter operating point upon these volumes, will be studied in order to understand how overall converter volume may be minimized. The principles behind semiconductor losses, a prime factor influencing converter power density, are demonstrated. Strategies for minimizing these losses are presented, with emphasis upon the utilization of alternate materials to accomplish this goal.

A. Modulation of DC Voltages

In order to control the flow of power within a MVDC distribution system, it is necessary to have modules which can raise and lower DC voltages. In a traditional 60 Hz AC terrestrial power distribution system, transformers are used to step up and step down bus voltage levels as required by loads. Transformers are able to take advantage of time-varying voltages to convert energy in electrical form to magnetic form through Faraday‟s Law and then back again to electrical energy at a new desired output voltage and current level (illustrated in Figure 3). Voltage levels in a MVDC distribution system, however, are constant; hence, the principle behind AC transformers cannot be used to convert voltage or current levels directly in an MVDC system.

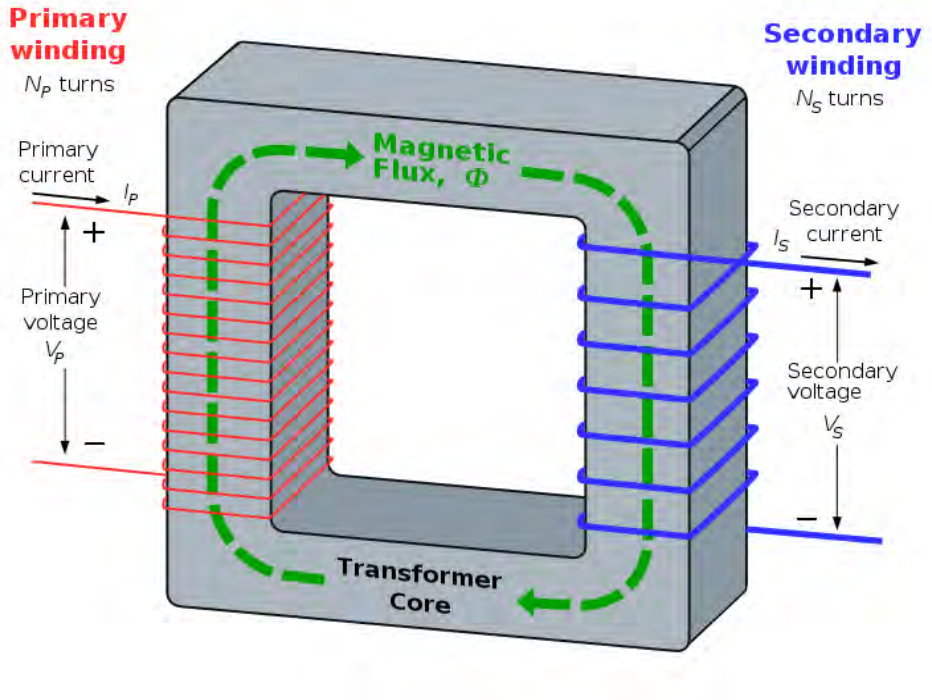

Figure 3 - Diagram Illustrating Principles of Transformer Operation

Due to the limitations imposed by the nature of a DC distribution system, it is necessary to employ an alternative method to change voltage and current levels. Although magnetics cannot directly be used to raise or lower voltage or current in a DC system, these levels can still be changed through switch action. This control method is known as switched-mode conversion. In switched mode conversion, switches are turned ON and OFF to convert the DC bus voltage to a quasi-rectangular waveform with the desired average value. The most basic circuit topology which accomplishes DC conversion is illustrated in Figure 4.

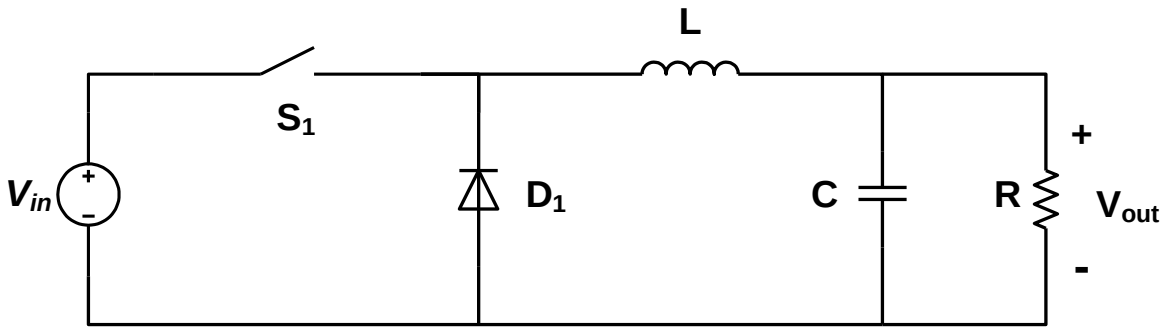

Figure 4 – Step-Down DC-DC Topology

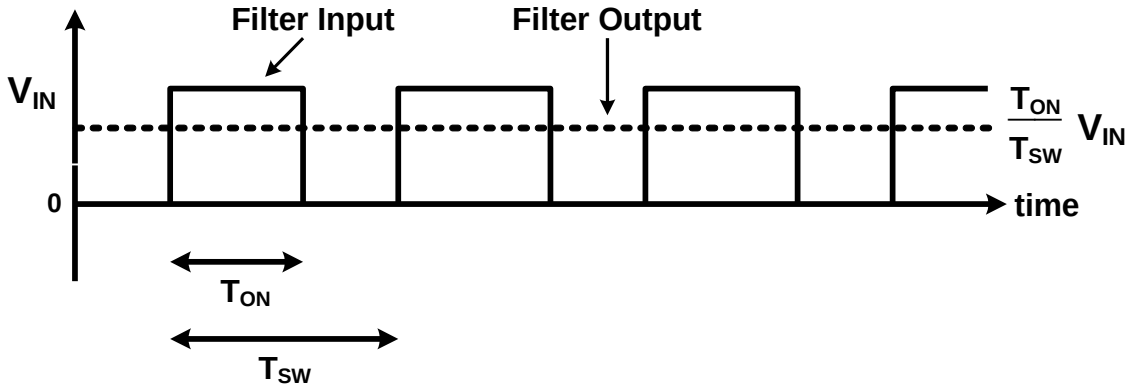

Figure 5 - Output of Voltage S1, D1 Pair

Through Fourier analysis of the voltage waveform of Figure 5, the steady-state output given by alternately switching S_1 can be broken down into its harmonic elements. The waveform can then be expressed as an infinite sum of sinusoids, a Fourier series, shown in Equation 1.

$$V_{Pulse} = A_0 + \sum_{n=1}^{\infty} A_n e^{jnw_0 t} \tag{1}$$

Examining the quasi-rectangular waveform in Figure 5, it is immediately apparent that it possesses a positive average value. This value is encapsulated in the coefficient A_0 in the Fourier series, and can be calculated as

$$A_0 = \frac{1}{T}\int_0^T V_{Pulse}(t)dt \tag{2}$$

where T is the switching period. If the waveform is as shown in Figure 5, we can calculate A_0.

$$A_0 = \frac{1}{T}\left[\int_0^{DT} V_{bus}\,dt + \int_{DT}^{T} (0)\,dt\right] \tag{3}$$

D is called the duty cycle. It is the ratio of the time S_1 is ON, divided by the switching period. Completing the integral,

$$A_0 = \frac{1}{T}\left[V_{Bus} DT\right] = DV_{Bus} \tag{4}$$

The average value A_0 is equal to the input voltage times the duty cycle. The voltage output of the switch-diode pair is then passed through a low-pass filter made up of and inductor L and capacitor C, appropriately tuned such that the corner cut-off frequency f_c is much less than the switching frequency f_{sw}. The filter effectively eliminates the harmonics within V_{Pulse}, allowing only the average value to pass to the output. Thus,

$$V_0 = A_0 = DV_{Bus} \tag{5}$$

Through modulation of the duty cycle, an output voltage anywhere between zero and the bus voltage may be produced. Other control variables, switching schemes and topologies may also be used to obtain voltage control. However, the underlying fundamental principle behind all DC-DC switched mode conversion remains the same, regardless of changes in the electrical topology or switching scheme. [10]

B. DC-DC Converter Power Density

For the purposes of this investigation, converter power density is a figure of merit of the overall power converter system. Converter power density may be defined as

$$\rho_{conv} = \frac{P_{Out}}{Vol_{Conv}} \tag{6}$$

P_{out} is the rated or maximum output power of the converter. Vol_{Conv} is the total volume of the converter, and is a sum of the volume of each converter component and the volume of coolant used within the converter. Power density provides a means for estimating the volumetric requirements of a given converter design, and allows for effective measurements of converter system volume when a converter is paralleled for higher system power throughput.

Since the inception of power electronic converters in the 1950s, converter power density has increased linearly by decade. A trend similar to Moore‟s Law for microelectronics, which predicts a doubling of components per chip every two years, is seen when power density figures in industry are plotted, shown below in Figure 6. Specifically, it has been seen that DC-DC converter power density, shown by the bold grey line, increases by an order of magnitude per decade. Projected estimates for the year 2020 following this trend predict an industrial DC-DC power converter density of 10 MW/m^3. [9] Given a power converter rated for a maximum throughput power of 10 kW, this power density figure predicts a volume of 0.001 m^3, equivalent to a 10 cm cube. Significant improvements must be made in current state-of-the-art power converter technology to reach predicted future power density goals.

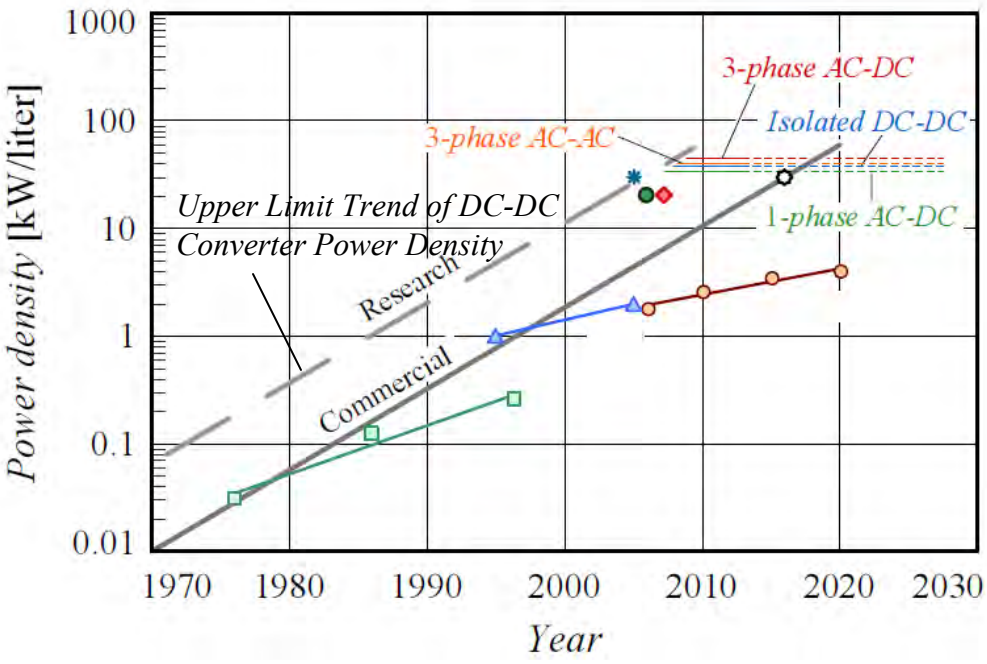

Figure 6 - Power Density Trends Over the Last Three Decades [9]

In order to understand how converter power density can be improved, it is necessary to appreciate the variables that affect converter power density for a given design. A power converter module is formed from five groups of components:

- Power Semiconductor Modules
- Control Circuitry
- Power Passive Components
- Cooling Systems
- Interconnection/Packaging

The first and second groups, power semiconductor modules and control circuitry, contain the semiconductor transistors that make up the switching elements of the power converter and the control circuit elements used to control switching. For a maximum current rating of 60A, a typical Si metal-oxide-semiconductor field effect transistor has a die area of 2 cm^2. Hence, semiconductor devices can be massively paralleled within a power converter with no significant penalty to converter volume from the size of the chips themselves. Circuitry within a switching control device today is small and power

dense. Although the semiconductor devices and their control form the primary electrical elements of a converter topology, power density is not significantly affected by either.

The three components of a power converter that require the largest volume are passive components such as capacitors and inductors used for filtering, isolation transformers, and cooling systems. The volume required of each of these components is a function of the switching frequency of the converter. The design methodology for capacitors and inductors is governed by the topology of the power converter in use. Returning to the example of the step-down converter discussed in the section above, values for the output inductor are chosen using the design relationships shown below in (7), where V_{out} is the output voltage, D is the duty cycle, Δi_L is the current ripple, and f_{sw} is the switching frequency. [10] The magnitude of the filter inductance is inversely related to the switching frequency of the converter.

$$L_f = \frac{V_{Out}(1-D)}{\Delta i_L f_{SW}} = \frac{K}{f_{SW}} \tag{7}$$

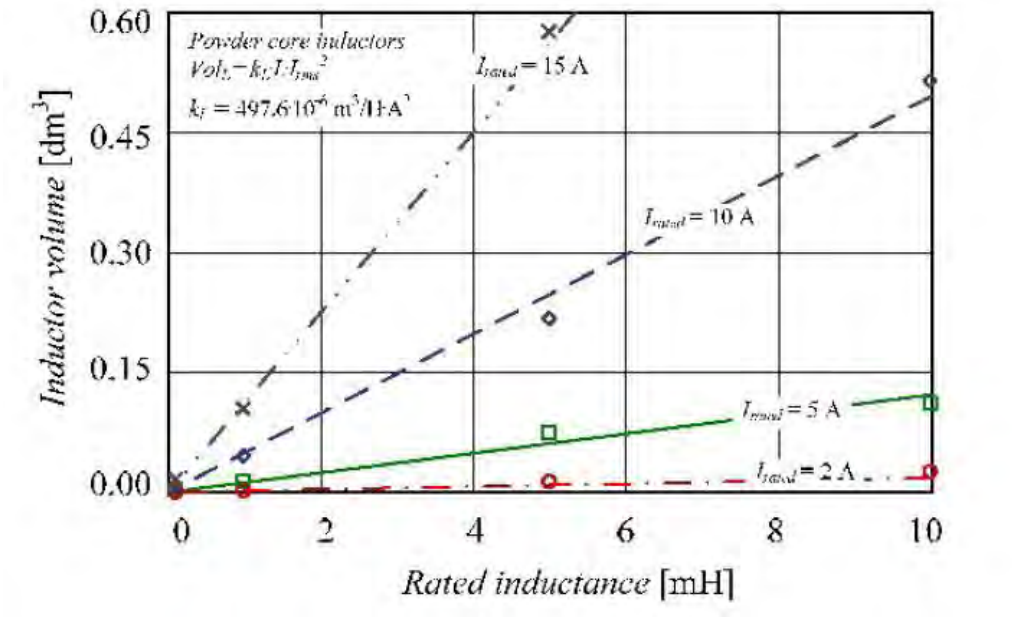

Figure 7 - Relationship between Inductor Volume and Inductance Value [9]

Surveying a range of commercially available filter inductors, Figure 7 shows the rough linear relationship between the values of the filter inductance and inductor volumes [9]. If switching frequency is increased, inductor volume decreases, increasing overall converter power density.

It would seem plausible that increasing switching frequency would decrease converter volume significantly, increasing converter power density. However, specific limitations upon maximum switching frequency occur due to increasing frequency related power losses within semiconductor switches and overvoltage and overcurrent effects that occur because of parasitic inductances and capacitances. Assuming that a converter is hard-switched, so that current and voltage change instantaneously across the switch, waveforms in Figure 8 are seen. V_{DS} is the voltage across the switch and I_D the current through the switching device.

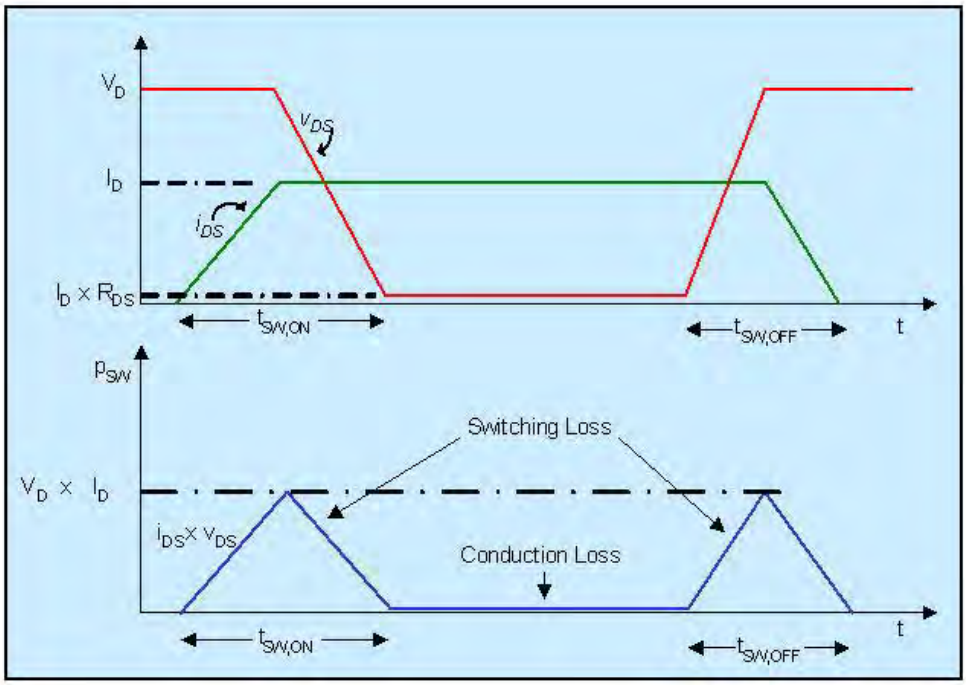

Figure 8 - Turn-on and Turn-off Switching Waveforms [10]

From these idealized waveforms, the following power loss relationship shown in (8) is derived by computing the average value of the product of the voltage and current waveforms.

$$P_{Loss} = \frac{1}{2} V_d I_d f_s (t_{on} + t_{off}) + P_{Cond}(P_o) \tag{8}$$

In (8), V_d is the off-state voltage, I_d is the on-state current, f_s is the switching frequency, and t_{on} and t_{off} are the switching turn on and turn off times. The times t_{on} and t_{off} quantify the amount of time it takes for the switch current and voltage to transition into the ON or OFF state. The $P_{Cond}(P_o)$ term is the conduction loss, dependent upon the type of switch being used. For magnetic filter components, losses are found using the Steinmetz relationship [10], shown below in (9),

$$P_{Loss,Trans} = kfB_{Max}^{n} \tag{9}$$

where B_{Max} is the maximum flux density in the core and k is a material dependent constant. Both semiconductor and magnetic losses increase linearly as switching frequency is increased. These losses manifest themselves as heat, which must be removed from the converter. Surface area, and hence volume, must be increased to tolerate increased heat levels. As frequency increases, reductions in converter volume from shrinking passive filter components begin to be overtaken by the increasing volume of the heat removal system. Though various heatsinking configurations and designs may be used to optimize heat removal, heatsink volume increases with switching frequency. Thus, for every converter design, there is a maximum frequency beyond which power density decreases significantly.

Given thermal limitations, it is necessary to find some way to decrease losses to increase maximum switching frequency, thereby increasing power density of future converters. There are several methods of accomplishing this goal. First, certain power converter circuit topologies exist in which one or more types of losses within the converter circuit may be reduced or eliminated. These topologies reduce stress upon circuit components and decrease component cooling requirements. Use of unipolar power transistor technology can additionally decrease losses. Metal-oxide-semiconductor field effect transistors (MOSFETs) have low switching losses and can tolerate high switching because of high conduction losses, which negate the benefit of reduced switching loss at high power. In order to increase the power rating of unipolar devices, such as MOSFETs, novel semiconductor materials must be used to decrease on-state resistances. It is expected that these materials will increase converter power density by an order of magnitude or more. [9]

To improve converter power density, semiconductor losses must be effectively minimized. It is informative to consider the typical magnitude which semiconductor device losses comprise total losses within a power converter. The power losses of a representative converter, constructed at ETH Zurich to optimize DC-DC converter power density and minimize heat sink volume, are broken down into groupings by loss element in Table 1. Semiconductor losses are clearly dominant in converter system losses, comprising over 80 percent of the total system loss.

Magnetics Losses [W]	MOSFET Switching Losses [W]	MOSFET Conduction Losses [W]	Rectifier Losses [W]
48.3	17.8	96.8	83.3

Table 1 - Loss Distribution in an Optimized DC-DC Converter [3]

C. Semiconductor Power Devices

As stated in the preceding section, greater system losses imply an increasing heat management volume and a corresponding decrease in power density. Thus, due to the dominance of semiconductor losses in representative systems, definitive gains in power density can be shown if semiconductor losses can be reduced. In order to understand how semiconductor losses may be decreased, it is necessary to understand the mechanisms through which power is lost in semiconductor devices. Power semiconductor transistors are large scale variations of similar devices used to create logic gates in digital circuits, effectively varying resistances within the circuit to create switching action. This is accomplished by using certain semiconductor materials, such as Silicon (Si). The properties of Si lie between those of insulating and conductive elements in the periodic table, and its conductance is highly sensitive to temperature. Semiconductors have crystalline properties at the microscopic level, shown in Figure 9 below. The displacement of an electron within this crystalline lattice, either through temperature increase or by „doping" the material with an ion that adds or removes an electron, changes the conductivity of the material.

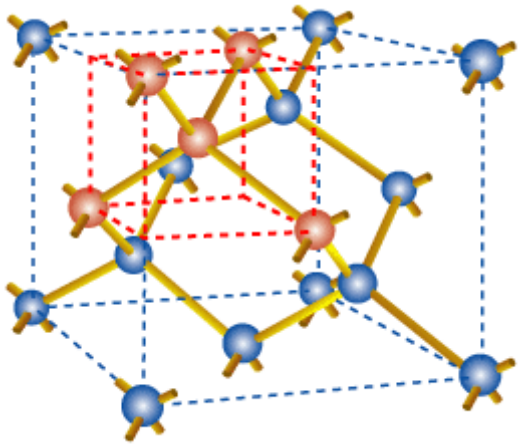

Figure 9 - Crystal Lattice Structure of Si [15]

Semiconductor devices are formed through various junctions of doped semiconductor material. The structure of these junctions determines how current can flow through the device. The device structure under study in this investigation is known as a metal-oxide-semiconductor field effect transistor (MOSFET), and has the structure shown in Figure 10. The MOSFET operates by creating an „inversion" region in the p-type semiconductor beneath the gate. Application of a positive voltage to the gate structure creates an n-type „channel" through which current flows. Due to the nature of the channel, MOSFETs are known as unipolar devices, as only one type of charge conductor flows through the device in the on state. Insulated Gate Bipolar Transistors (IGBTs), an alternative form of transistor, form the core of the grouping known as bipolar devices, as both electrons and holes, flow during the on-state of the device. Accumulated charge in bipolar devices must be removed at turn-off, decreasing their efficacy at high switching frequencies. A comparison of switching times between a MOSFET and an IGBT at similar ratings is shown below in Table 2. [15] MOSFETs are favored for high switching frequency applications, making them the prime semiconductor device used in studies of converter power density optimization.

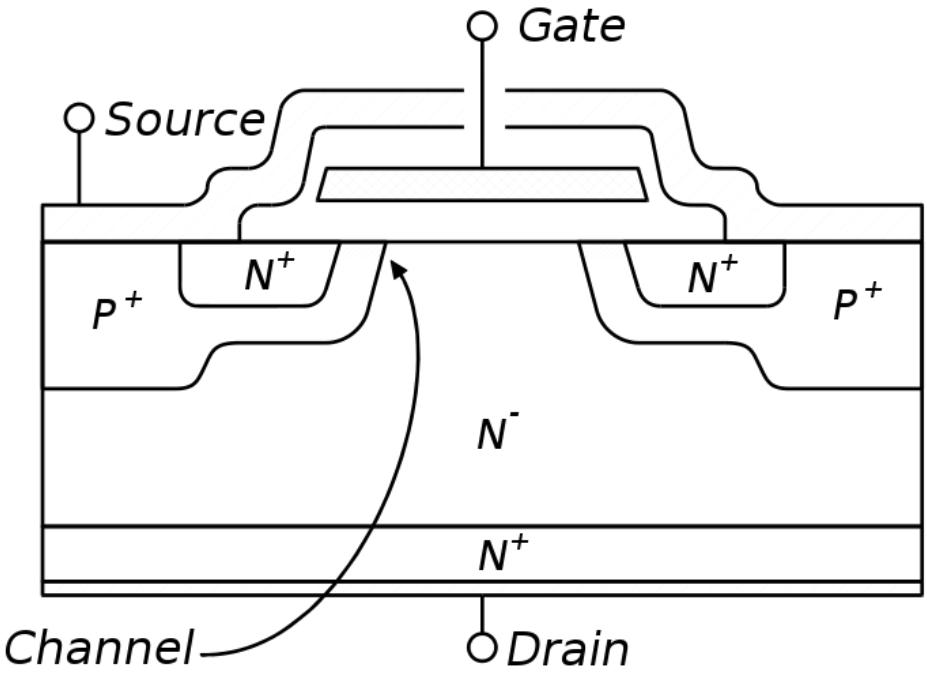

Figure 10 - Power MOSFET Internal Structure

Device Ratings – 600V, 10A	t_{sw}
Power MOSFET	50 ns
Power IGBT	100 ns

Table 2 - Comparison of Switching Times between a PowerIGBT and MOSFET [15]

The current-voltage (IV) characteristic of the MOSFET, shown in Figure 11, can be derived by analyzing the quantum properties of the device. As depicted on this diagram, the MOSFET possesses three regions of operation: cutoff, linear and saturation. When the voltage V_{GS} applied across the gate terminal of the device is less than the threshold voltage V_t, the devices remains in the cutoff region and no current flows. In the linear region, the voltage across the drain to source terminals V_{DS} remains at a level such

that $V_{DS} < V_{GS} - V_t = V_{DS,sat}$, where voltage V_{DS} is proportional to the current through the device I_D. If $V_{DS} > V_{GS} - V_t = V_{DS,sat}$, the MOSFET is in the saturation region, and the device functions as an amplifier of the V_{GS} signal.

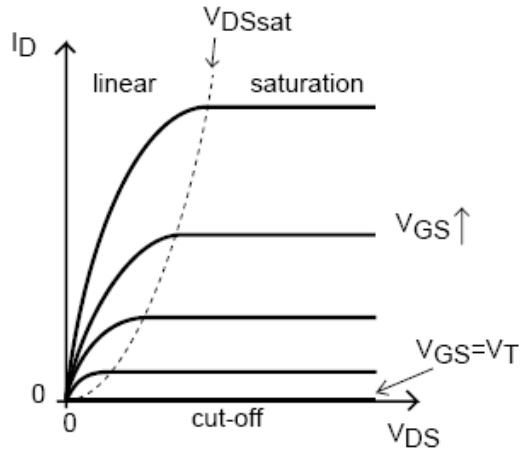

Figure 11 - MOSFET Current-Voltage Characteristic [15]

D. MOSFET Loss Mechanisms

In a power electronic circuit, the MOSFET operates in the cutoff and linear regions, known as the commutating states. Power loss within the MOSFET can be formulated as the product of V_{DS} and I_D. If a circuit using a power MOSFET operates the device in each state, the power losses within a MOSFET can be broken into the losses due to linear „on" state and the transition losses between the „on" state and the cutoff state, known as switching losses.

$$P_{Loss,MOSFET} = V_{DS} I_D = P_{Loss,Linear} + P_{Loss,Switching} \tag{10}$$

Since in the linear „on" state, the current through the MOSFET I_D is proportional to the voltage across the device V_{DS}, the relation between I_D and V_{DS} becomes

$$V_{DS} = R_{DS,On} I_D \tag{11}$$

where $R_{DS,On}$ is the effective resistance of the conducting path through the MOSFET in the on state. Hence, the power losses in the linear on state may be expressed as

$$P_{Loss,Linear} = I_D^2 R_{DS,On} \tag{12}$$

The $R_{DS,On}$ factor is a sum of the effective resistances of different regions of the current path through the MOSFET. This is shown graphically in Figure 12.

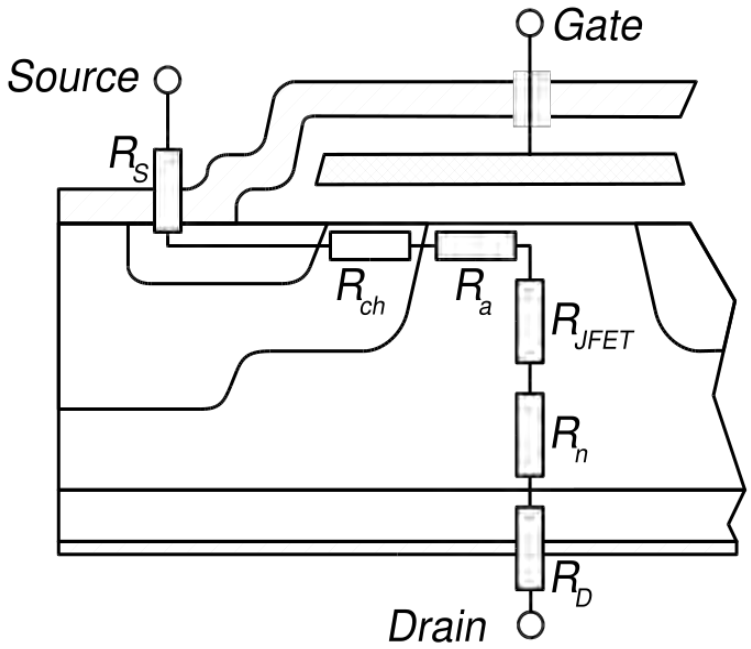

Figure 34 - Power MOSFET On-state Resistances [1]

$$R_{DS,ON} = R_S + R_{ch} + R_a + R_{JFET} + R_n + R_D \tag{13}$$

In Equation (13), R_s is the resistance due to the source diffusion layer, R_{ch} is the resistance due to the inversion channel, R_a is the resistance due to the accumulation of charge within the inversion layer, R_{JFET} is the resistance due to the Junction FET (JFET) structure within the MOSFET, R_n is the drift layer resistance, and R_D is the resistance due to the drain diffusion layer. In order to block the voltage magnitudes required in a power circuit, a layer known as the epitaxial layer must be placed within a power MOSFET

structure to increase the voltage breakdown level of the device. The resistance of this layer, R_{Epi}, consisting of R_n, R_{JFET}, and R_a, dominates the on-state resistance of the device at higher levels of rated blocking voltage. Channel resistance also contributes significantly to on-state resistance; however, R_{ch} can be minimized by applying a significantly large V_{GS} voltage to the gate to maximize the width of the channel. The resistance of the epitaxial layer is influenced by its width and its doping level. To block higher voltage levels, the depth of the layer must be increased and doping level decreased. An analysis of Si power MOSFETs by Biela in [1] has demonstrated the following relationship between device breakdown voltage and specific on-state resistance shown in (14). The specific on-state resistance, $R_{on,sp}$, the on-state resistance normalized by die area, of Si MOSFETs is graphed below versus breakdown voltage in Figure 13.

$$R_{ON,Sp} = 5.83 \times 10^{-9} \left(BV\right)^{2.5} \tag{14}$$

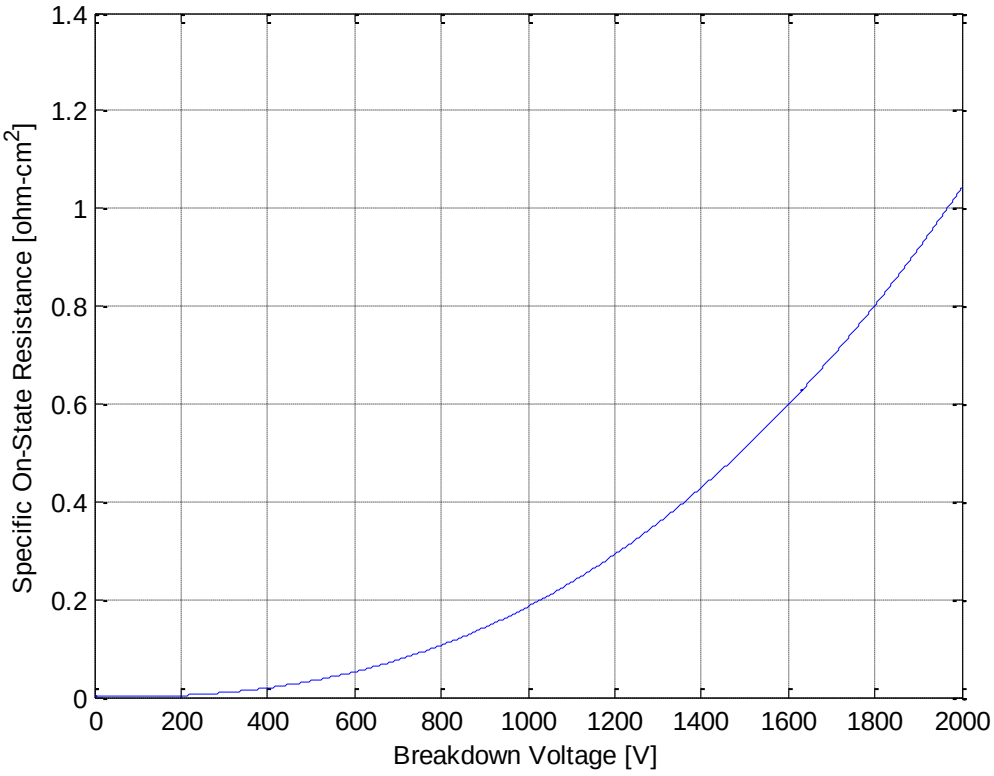

Figure 13 - Si MOSFET On-state Resistance versus Breakdown Voltage

Power devices that use Si as the semiconductor material for fabrication are limited by a maximum operating temperature that is a function of the packaging technology of the device. Assuming that on-state losses dominate the losses of the MOSFET, a safe-operating area (SOA) shown below in Figure 14 can be derived. MOSFET devices made from Si have a maximum rating of about 1000 V and 100 A. [10] Beyond these ratings, bipolar devices such as Insulated Gate Bipolar Transistors (IGBT) are favored for use. Converters using MOSFETs as commutating devices are restricted in maximum possible power throughput by this limitation.

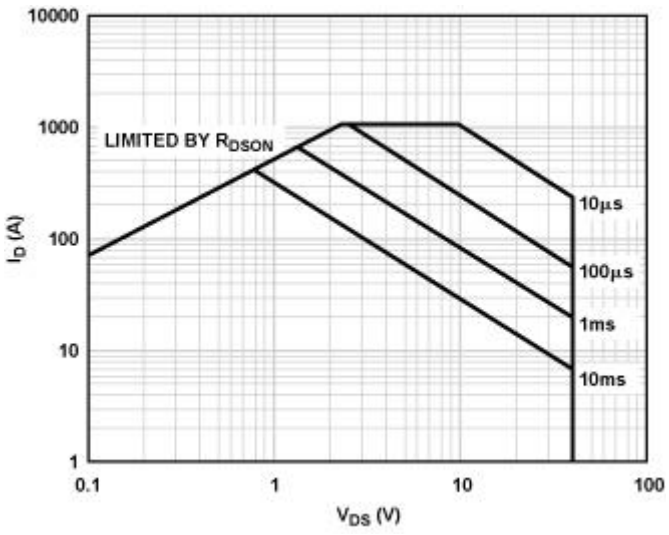

Figure 14 - 1000V, 40A MOSFET Safe Operating Area

On-state resistance and losses may be decreased by increasing the MOSFET die area, A_D. However, a tradeoff exists between A_D and the switching loss of a MOSFET which holds the maximum rating of the devices within the SOA shown above. The structure of the MOSFET contains three intrinsic capacitances, $C_{GS,}$ C_{GD} and C_{DS}, which limit the rate of voltage rise dV_{DS}/dt and the rate of current rise dI_D/dt through the device. Since dV_{DS}/dt and dI_D/dt are finite, finite time is required for both I_D and V_{DS} to rise or fall to their steady-state values. Assuming that times t_{on} and t_{off} are required to turn on and off the device, Equation (8) holds for the switching losses. Further examination of the turn-on and turn-off characteristics of the MOSFET demonstrates the influence of the $C_{GS,}$ C_{GD} and C_{DS} upon transient performance. As charge is supplied to the gate terminal of the MOSFET, the voltage across the gate V_{GS} rises until it surpasses V_T, the threshold voltage of the device. At this point, the device conducts. However, C_{GD} must be charged in order to fully bias the MOSFET into the on state, forcing V_{GS} to plateau at a level known as the Miller voltage. The length of time the voltage spends at this level is determined by the nonlinear characteristics of the magnitude of C_{GD}. After charging C_{GD}, voltage levels

rise within the MOSFET to their steady-state values as C_{DS} is fully charged. The effects of these capacitances determines the total rise-time of the device and hence the total switching losses. Increasing die area increases the intrinsic capacitances of the MOSFET, effectively transferring decreases in power losses in the on-state to switching losses in the transition period. This tradeoff, in turn, decreases the power rating of the device. [15]

Multiple strategies exist to decrease both MOSFET on-state and switching losses. As stated above, there is a seemingly insurmountable tradeoff between a decrease of on-state losses and switching transient losses, due to the increase of intrinsic device capacitances with increasing die area. This tradeoff places an upper limit on device operating frequency for a given maximum voltage and current rating. However, novel solutions exist which take advantage of the geometry of the gate region to counter increases of intrinsic capacitances with increasing die area, such as the International Rectifier HEXFET [10]. State-of the art Si MOSFETs currently make use of an architecture known as an epitaxial super-junction structure, in which region of horizontally alternating p-type and n-type silicon layers are used for the epitaxial region. Using alternating layers decreases the doping levels required for a given breakdown voltage rating, simultaneously decreasing $R_{DS,On}$ values. However, though these device architectures increase some MOSFET capability, current MOSFET technology is inherently limited by an upper bound imposed by the physical capabilities of the device material, Si. A study by Park in [18] has analytically derived the upper bounds of current Si MOSFET technology, shown graphically in Figure 15. The lower limit of on state resistance in Si super-junction technology is shown as the bottommost dotted line in

Figure 15. In order to increase the maximum power throughput capabilities of converters using MOSFET technology, it is necessary to explore MOSFETs fabricated from materials that possess superior capabilities to Si in the high power regime.

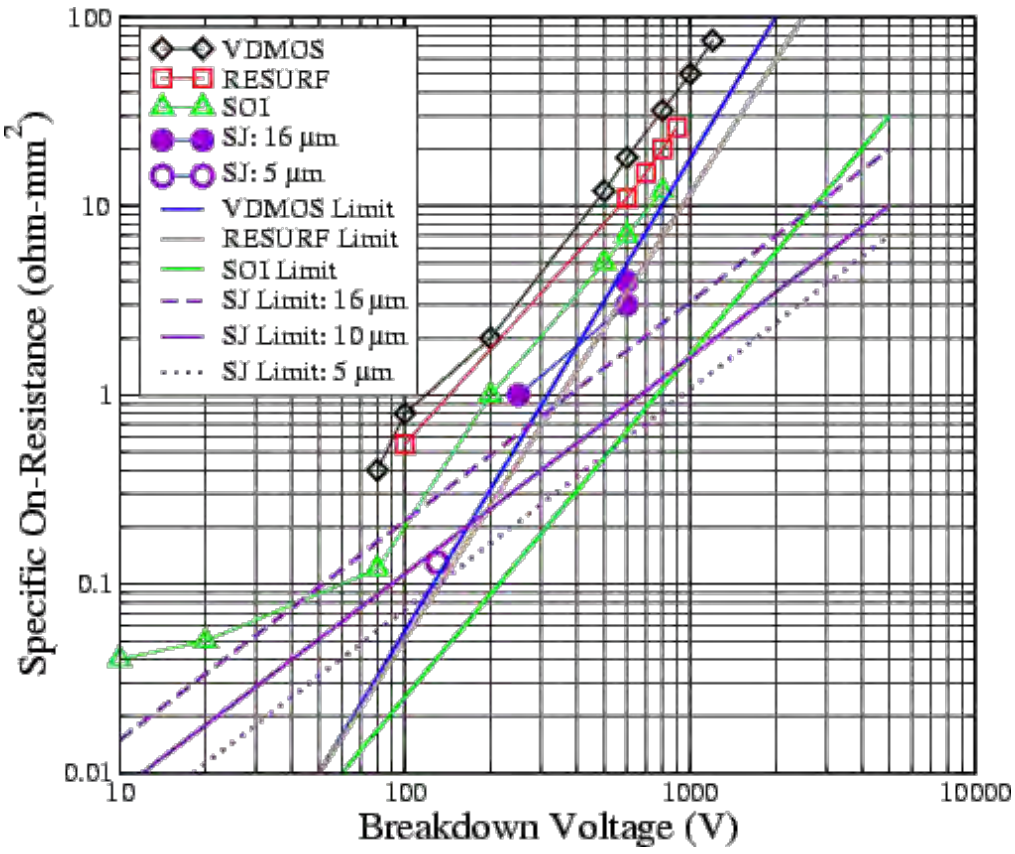

Figure 15 - MOSFET Technology On-state Resistance Limitations [18]

E. Wide Bandgap Semiconductors and Power Density

The upper boundary of the rated power throughput of power MOSFETs is created by both the thermal limitations and the electrical properties of Si material. Material properties of Si are listed in Table 3. The bandgap energy of the semiconductor, E_G, plays a critical role in the thermal performance of the semiconductor. This can be shown analytically through Equation (17), which describes the concentration of excited carriers in a sample of pure semiconductor material. [15] In Equation 17, T is the temperature, k_B is Boltzmann"s constant, E_G is the bandgap, and A is a constant dependent upon the crystallographic properties of the material.

$$n_i = AT^{3/2} \exp\left(-\frac{E_G}{2k_B T}\right) \tag{17}$$

As temperature T increases, the concentration of carriers increases. Beyond a concentration of 10^{18} cm^{-3} carriers, intrinsic or otherwise, Si effectively functions as a pure conductor. [15] Even a slight increase in carrier concentration beyond its nominal value at room temperature can completely change the operation of a semiconductor device, leading it to breakdown at voltages significantly lower than the nominal blocking voltage. A larger magnitude of bandgap, E_G, delays the onset of this transition. This delay effectively increases maximum device operating temperature. The critical electric field strength E_C of a material can be additionally derived from the value of E_G. This value governs the necessary thickness of the epitaxial drift layer for a desired breakdown voltage rating of a MOSFET fabricated with Si. Equation (14) in the previous section is derived from these material properties. Specific on-state resistance, width of the drift depletion region and required doping levels are given for a range of rated Si MOSFET

breakdown voltages in [6]. Examining these relationships, a MOSFET rated for 1200V breakdown fabricated with a 1.0 cm^2 die area can be seen to have an on-state resistance of 0.29 Ω. The maximum power rating of a MOSFET can be effectively communicated as the product of the maximum rated current and voltage, known as the apparent power rating. Beyond this power range, bipolar devices are favored for an application due to their significantly lower conduction losses, introducing limitations upon maximum converter switching frequency and consequently converter power density.

	Si	4H-SiC	6H-SiC
Bandgap, E_G [eV]	1.10	3.30	3.00
Critical Electric Field, E_C [MV/cm]	0.25	2.20	2.50
Thermal Conductivity, k [W/cm.K]	1.50	5.00	5.00
Melting Point (C)	1420	2830	2830
Electron Mobility, μ_n [cm^2/V.s]	1350	947	380
Hole Mobility, μ_p [cm^2/V.s]	480	120	80

Table 3 – Material Properties of Si, 4H-SiC and 6H-SiC [15],[6]

To surmount this upper limit upon apparent power ratings of a device, it is necessary to investigate materials that can overcome the inherent physical limitations of Si. Silicon Carbide (SiC) is a prime material for fabrication of MOSFET devices with improved loss performance. SiC is known as a wide bandgap material due to its typical value of E_G of around 3.0 eV. Wide bandgap materials are defined as materials with bandgaps greater than 2 eV. As shown in Equation (17), this increase in bandgap energy helps lead to a higher maximum operating temperature. A MOSFET fabricated with 6H-SiC, a crystal structure of SiC commonly used in semiconductor manufacture, possesses an effective maximum operating temperature of 300 ºC using current device packaging

technology, twice that of a device fabricated from Si. [11] A converter employing devices fabricated from wide-bandgap materials, such as SiC, can therefore handle higher losses, translating into higher potential converter output power for a given design.

MOSFETs fabricated with SiC experience lower conduction losses than Si, due to a critical electric field breakdown value of 2.50 MV/cm. An increase in E_C allows for a thinner drift region within a MOSFET structure, translating to a smaller specific on resistance value for a given breakdown voltage rating. Baliga in [1] formulated a method for calculating on-state resistance in a MOSFET structure, using an analysis of the device similar to that laid out in the previous section. Table 4 shows $R_{on,sp}$ values calculated for various device breakdown voltage ratings fabricated with 6H-SiC and Si.

Breakdown Voltage, BV [V]	6H-SiC, MOSFET $R_{on,sp}$ [ohms.cm^2]	Si, MOSFET $R_{on,sp}$ [ohms.cm^2]
200	1.69×10^{-5}	3.35×10^{-3}
1000	6.11×10^{-4}	1.88×10^{-1}
3000	8.20×10^{-3}	2.92×10^{0}
5000	2.95×10^{-2}	1.05×10^{1}

Table 4 - $R_{sp,on}$ versus Breakdown Voltage for 6H-SiC and Si MOSFETs [1]

For a rated breakdown voltage of 3000V, a MOSFET fabricated with SiC has an $R_{on,sp}$ value that is 305.7 times less than that of a MOSFET fabricated with Si. Assuming that on-state losses dominate the losses of the MOSFET and realizing that on-state losses are directly proportional to $R_{on,sp}$, power converters utilizing SiC MOSFETs will experience vastly increased efficiency at higher power levels in which high current levels are used. Given a maximum allowable device junction temperature, this efficiency again translates into higher power density for a given design.

Kolar in [9] demonstrated directly the relationship between semiconductor device capabilities and power density of a converter design. The study in [9] explored the optimization of the power converter design process with respect to power density. In the study, the volume of the optimal heatsink required to dissipate the losses of the semiconductor device was found to be inversely related to the maximum permissible junction temperature. This relationship is shown in Equation (20), where $T_{J,Max}$ is the maximum junction temperature, $R_{th,J\text{-}S}$ is the thermal resistance from the junction to the sink and η_{sys} is the system efficiency. K is a constant related to the architecture of the heat sink.

$$Vol_{cs} = K\left(\frac{T_{J,MAX} - T_{ambient}}{P_{OUT,Converter}\left(\eta_{SYS}^{-1} - 1\right)} - \frac{1}{2}R_{th,J-S}\right)^{-1} \tag{20}$$

Assuming that the output power, $P_{OUT,Converter}$, of the converter and the thermal resistance $R_{th,J\text{-}S}$ from the device junction to the heatsink are constant, then the volume decreases with higher junction temperatures and system efficiencies. Manipulating this equation, we find

$$\frac{P_{OUT}}{Vol_{cs}} = \rho_{Heatsnk} = \frac{1}{K}\left(\frac{T_{J,MAX} - T_{ambient}}{\left(\eta_{SYS}^{-1} - 1\right)} - \frac{1}{2}R_{th,J-S}P_{OUT}\right) \tag{21}$$

If we assume that system power losses are dominated by semiconductor losses, this relationship demonstrates that the power density of the thermal management system, and hence the power density of the system, increases if a semiconductor device is used that can tolerate a higher junction temperature and possesses lower losses is used. Devices fabricated with SiC, therefore, should demonstrate an increase in power density for a given converter design.

III. Power Density Testing Procedure and Methodology

If the maximum allowable junction temperature of a device is increased in a power converter design, Equation (21) states that volumetric requirements for the device heatsinking apparatus decreases. If heatsinking volume is kept constant, then increasing power results in increasing junction temperature. Thus, a converter with constant heatsink volume may be used as a testbed to compare the power density performance of two types of MOSFET technology by measuring the power throughput of the converter allowed by each technology for a given maximum allowable junction temperature.

The NGIPS roadmap envisions a power converter module called the PCM-1A (Power Conversion Module) within the MVDC architecture that links load banks to the power distribution bus. [7] The module is required to interface power from the medium voltage DC bus, supplying multiple loads with varying supply voltage requirements. [7] It is expected that power demand from the PCM-1A will approach multi-megawatt levels. To reach high levels of power throughput, a PCM-1A module may consist of multiple paralleled DC-DC converters of kW range rating, known as Ships Service Converter Modules (SSCMs). In order for power density of the PCM-1A to increase, SSCMs must be volumetrically optimized for their power throughput rating.

Current technology enables the power density of a PCM-1A design to reach a nominal power density of 1 MW/m^3. [4] A 300 kW SSCM with this power density rating will have an effective volume of 0.3 m^3, equivalent to a 67 cm cube. The Office of Naval Research (ONR) has proposed a target of 3 MW/m^3 as a desired converter power density rating before technology deployment, a 300 percent increase above current converter power density levels. [4] SSCM modules can be created which reach this standard using

SiC semiconductor device technology. By testing a static SSCM design using Si and SiC devices, appropriate gains in power density can be directly demonstrated and an avenue to an achievement of SSCM ONR power density goals explored.

This chapter explores the principles and methodologies used to test converter power density. In Section A, a principle known as thermography is introduced and explored for use in measuring device junction temperature. In Section B, the testing methodology used to test power density is reviewed. Power density is measured by measuring junction temperature, and specifying the rated power of the tested converter by the operating point at which the junction temperature reaches a maximum allowable magnitude.

A. Thermographic Testing

In order to characterize converter power density, the output power of the converter at which the junction temperature of the devices under test reached a value of 100 ºC was measured. A junction temperature value of 100 ºC was chosen as a reasonably high junction temperature at which power density gains offered by SiC would become apparent. To accomplish this, junction temperature of the devices must be measured during steady-state converter operation. Multiple methods of measuring the temperature of a surface have been explored in past research, using thermocouples or thermistors attached to a measured surface. [13] However, these methodologies are generally inaccurate and unwieldly for measuring surface temperatures greater than 100 ºC [13].

Dr. Thomas Salem, at the Army Research Laboratory (ARL), explored a thermographic principle for measurement of device junction temperatures in [13]. In this method, an infrared camera is used to measure infrared radiation emitted from the device die surface. The emissivity coefficient of the surface is used to estimate the surface temperature of the device junction. Because various materials with varying coefficients of emissivity are present at the measured surface, it was found that an applied surface coating was needed to make the surface emissivity coefficient uniform to obtain accurate measurements. Measurement of the surface temperature of a MOSFET die is plotted using the thermographic method along with the true temperature of the block, measured using a thermocouple in Figure 16. Using a coating of Boron Nitride to equalize emissivity, surface temperatures were found to correspond to within 1 percent of their true values using infrared measurement.

-5.00

Figure 16 - Temperature Error for Die Temperature of MOSFET [13]

This study adopted the thermographic method to measure device junction temperature during steady-state converter operation. Settings for the infrared measurement were adopted from those found in [13], and devices were prepared using the Boron Nitride coating thickness prescribed in the study.

B. Testing Procedure

The primary goal of converter testing was to directly measure the junction temperature of the MOSFETs under steady-state conditions. Converter power density was characterized by determining the output power level at which a MOSFET junction temperature of 100 °C was reached. In order to measure junction temperature, the semiconductor die of each device was to be fully exposed. Since the Si FETs were packaged, chemical processes which would de-encapsulate the semiconductor die were explored. However, it was found during the de-encapsulation process that the electrical characteristics of the Si-FETs had changed enough to result in a detrimental imbalance in the operation of the converter, quickly leading to thermal runaway and destruction of the de-encapsulated device. Instead, an alternative method was used to measure junction temperature. An average FET heat sink temperature, T_S, was measured using the FLIR infrared camera. Knowing the thermal resistance from the heat sink to ambient and measuring the ambient temperature (T_A), the device average power loss can be estimated.

$$P_{loss} \approx \frac{T_S - T_A}{R_{\theta,SA}} \tag{39}$$

The junction temperature can then be approximated from estimates of the remaining thermal resistances as follows from the simplified thermal model shown in Figure 17. [10]

$$T_J \approx T_S + P_{loss} \times \left(R_{\theta,CS} + R_{\theta,JC} \right) \tag{40}$$

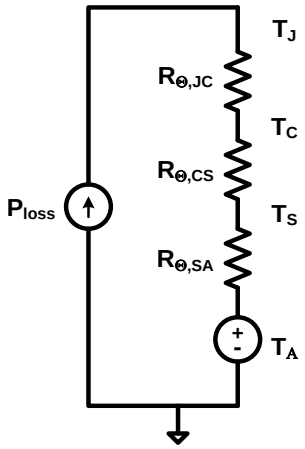

Figure 17 – Electrical Equivalent Model of MOSFET Heatsink Thermal Pathway

A load bank was set to a desired output load resistance and thus a desired output power. The duty cycle was set to a constant value chosen by the resolution in the change in output power required between load steps. The mounted IR camera was positioned to monitor the device temperature. The low-voltage gate driver power supply was energized and set to 15V. A high-power DC power supply was powered and set to 200V. Cooling fans were powered up, providing airflow across the heatsink. Control circuitry was then made to initiate the five-second ramp up to the prescribed duty cycle.

For each operating point, converter waveforms relevant to the turn-on and turn-off process are captured and stored on an oscilloscope. The transformer primary voltage and current are measured as well as the transformer secondary voltage. The converter input

and output voltages and currents are measured. For the first operating point, the converter is allowed to achieve thermal equilibrium (~30min), with the elapsed time interval being used to estimate a thermal time constant (~5.89min). This thermal time constant is then applied to subsequent measurements to estimate final temperatures after running the converter for ~7min. The load bank is stepped at approximately 200W levels. The maximum power throughput is determined when the junction temperature of the device under test reaches 100 ºC.

IV. Testbed Converter Design

In order to successfully test and compare power density gains between Si and SiC MOSFETs, a power converter „testbed" must be designed and constructed. Volume of the converter is held static between testing of the Si and SiC devices. This chapter covers the design of this „testbed" converter. Section A covers the selection of the topology of the converter. Section B reviews the selection of design constraints for the converter, chosen to be representative of a prototype NGIPS system. Remaining sections cover the selection and design of various converter components, and their integration into a full converter assembly.

A. Single Active Bridge Topology

In order to fulfill the requirements of the NGIPS MVDC power distribution system design, it is necessary to provide galvanic isolation between the power bus of the shipboard power distribution system and the bus supplying the load. Isolation is necessary because a fault across a load that is not isolated from the power bus will short the bus to ground, disabling not only power flow to the load but throughout the power system as a whole. Galvanic isolation is provided when the power flowing through a converter module supplying the load is converted to a form other than electrical energy before being transformed back to electrical energy to supply the load. This allows for fault protection of the power bus, improving fight-through capability of the power distribution system, graphically illustrated below in Figure 18.

Figure 18 - Illustration of Galvanic Isolation Protection [7]

For high power applications, galvanic isolation is most often provided by a transformer, which uses the principle of Faraday‟s Law to convert time-varying electrical energy into magnetic energy and then back to electrical energy on its secondary side. The design phase of this project was initiated by a study into various topologies incorporating galvanic isolation.

A study in [3] surveyed three galvanically isolated converter topologies to determine which maximized overall converter power density. These topologies, known as „soft-switched‟ topologies, were chosen because they minimized or eliminated switching losses within the converter through placement of reactive elements within the converter or by modulation of the switching schemes of the semiconductor switches. It was found that the topology shown below in Figure 19, known as the Single Active Bridge (SAB) topology offered the smallest tradeoff between component count, required

volume and theoretical switching losses for a desired converter output power. From the results of [3], the SAB topology was also chosen for the design of the converter testbed.

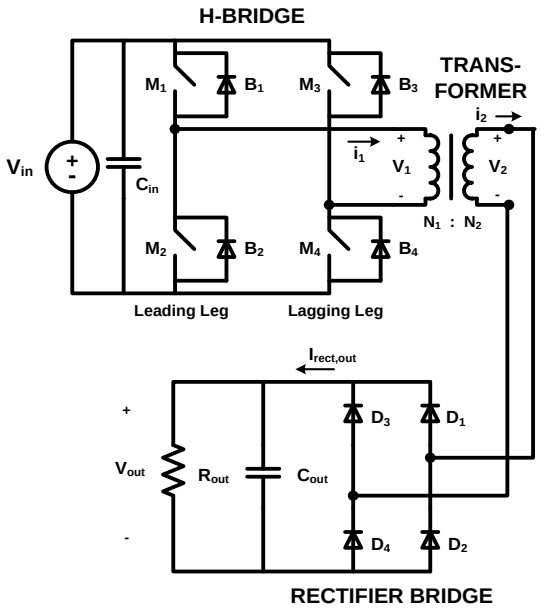

Figure 19 - Single Active Bridge Topology

The SAB topology may be viewed as three separate subsections, as labeled in Figure 19. The first section, a phase shifted H-bridge inverter, consists of four semiconductor switches in an H bridge layout. The H-bridge transforms DC voltage at the input into an AC voltage by switching through a pre-determined switching scheme, which will be discussed in a following section. The second inverter stage outputs an AC waveform that is fed into a high-frequency (HF) transformer, providing galvanic isolation within the converter. Finally, the output from the transformer is fed into an H-bridge rectifier, which rectifies the AC waveform from the HF transformer and provides a DC output voltage which is filtered by the output capacitor.

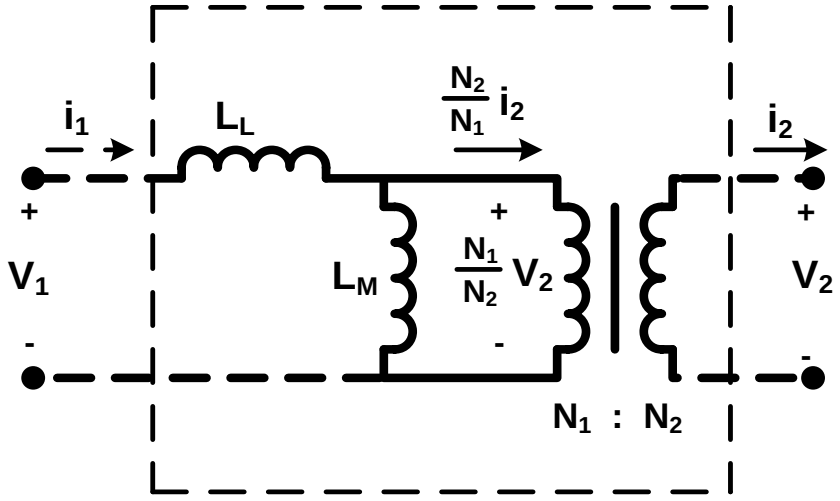

Figure 20 - High Frequency Transformer Model

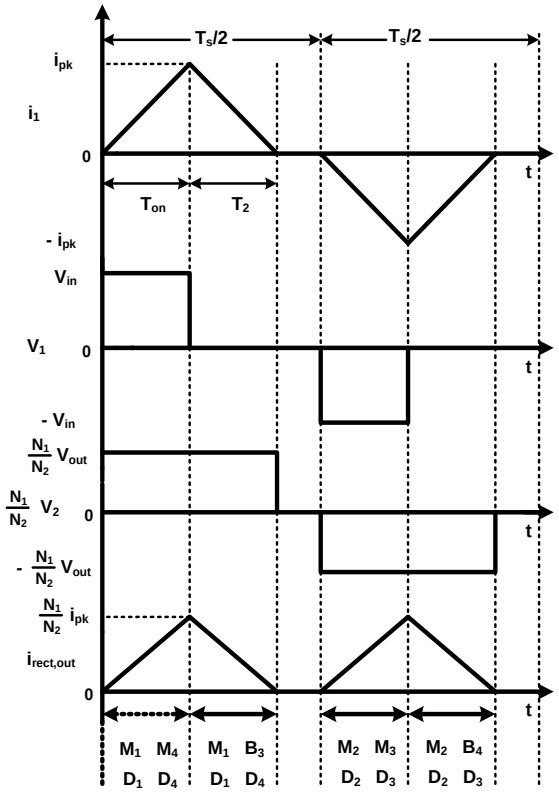

Figure 21 - SAB Steady-State Waveforms

Due to the lack of a filter inductor at the output, the SAB topology operates in discontinuous conduction mode (DCM) operation at all power throughput levels. Discontinuous mode is defined as the operating mode where the output current reaches

zero before the end of the switching period. Instead, the leakage inductance of the transformer, L_L, determines converter behavior. A simplified model of the transformer is shown in Figure 20. An analysis of the operation of the converter in DCM is determined by analyzing the waveforms given in Figure 21. In this analysis, it is assumed that the magnetizing inductance of the transformer, L_M, is significantly larger than L_L. Operation of the converter is divided into two half periods, demarked by the time $T_s/2$, shown in the waveforms of Figure 21. The first half of the cycle of operation begins when switches M1 and M4, shown in Figure 19, are gated ON with a zero current transition. This zero current transition enables both switches to turn on with no switching loss. At this point, the primary current i_1 begins to rise, biasing the rectifier diodes D1 and D4 on. The difference between the input voltage and the reflected output voltage appears across the leakage inductance, causing current i_1 to rise linearly to the value i_{pk} over time T_{on}. The time T_{on} is a control parameter. Assuming the transformer turns ratio to be $N = N_1/N_2$, the value of i_{pk} is found to be

$$i_{pk} = \left(V_{in} - NV_{Out}\right) T_{ON} / L_L \tag{22}$$

At the end of the T_{on} interval, MOSFET M4 is gated off. The primary current is still positive, and biases the free-wheeling diode B3 on. The voltage across the primary is zero in this interval, and the reflected output voltage across the leakage inductance causes i_1 to fall to zero by time T_2. At the end of this interval, switch M4 is gated off at zero current. The second half cycle begins at $T_s/2$, and initiates when switches M2 and M3 are gated on. Diodes D2 and D3 are turned on, and the output voltage reflected across the leakage inductance is $-V_{out}$. Current i_1 falls to the value $-i_{pk}$ in a time interval T_{on}. At the end of this interval, switch M3 is gated OFF and the freewheeling diode B4

begins to conduct. During this interval, the current begins to rise, reaching zero in a time interval T_2. The relationship shown in Equation (23) must hold between $-i_{pk}$ and T_2 if the converter is operating in DCM.

$$-i_{pk} = -NV_{out}T_2 / L_L \tag{23}$$

By summing (22) and (23), we can derive the required fall time T_2, shown below in Equation (24).

$$T_2 = \left(\frac{V_{IN}}{NV_{OUT}} - 1 \right) T_{ON} \tag{24}$$

The average current $i_{rect,out,ave}$ is found by integrating the rectified current $i_{Rect,out}$, shown in Figure 21, and dividing by the half period, $T_s/2$.

$$i_{rect,out,ave} = \frac{\frac{1}{2} N i_{pk} \left(T_{on} + T_2 \right)}{T_S / 2} \tag{25}$$

Since the filter capacitor C_f must have zero average current in steady state, only the average current flows through the load resistance. Hence, the output voltage is given by

$$V_{OUT} = i_{rect,out,ave} R_{OUT} \tag{26}$$

If the converter duty cycle is defined as $D = T_{on}/(T_s/2)$, then the required D given a specified converter operating point defined by $V_{IN,}$ $V_{OUT,}$ and f_{sw} can be derived. By substituting (23) and (24) into (25) and using the result in (26), the necessary duty cycle is

$$D = \sqrt{\frac{4L_L f_s}{\left(\frac{V_{in}^2}{V_{out}^2} - \frac{N_1}{N_2} \frac{V_{IN}}{V_{OUT}} \right) R_{OUT}}} \tag{27}$$

Hence, if we wish to increase the power level by decreasing the load resistance, we must increase the duty cycle in order to regulate the output voltage level. We can use this relationship to derive operating points which give a desired range of output power levels at which to test converter operating characteristics.

In order to maintain the operation of the converter in DCM, the current i_1 must be allowed to return to zero before the end of the half cycle. If we express this requirement mathematically and utilize the expression for T_2 derived previously, we can derive the following constraint upon duty cycle within DCM operation.

$$D < \frac{N_1}{N_2}\frac{V_{out}}{V_{in}} \tag{28}$$

If (28) is plugged back into (27), and recognizing that $R_{out} = V^2_{out}/P_{out}$, the value of P_{out} at the boundary of DCM is derived as

$$P_{out,dcm} = \frac{V_{out}^2 N^2 - \left(V_{out}^3 / V_{in}\right) N^3}{4 L_L f_s} \tag{29}$$

To calculate the optimal turns ratio, the derivative of (29) is taken and set it to zero to get the following relationship.

$$N_{opt} = \frac{N_1}{N_2} = \frac{2}{3}\frac{V_{in}}{V_{out}} \tag{30}$$

This relationship can be substituted into (29) to get the maximum power output that the converter can maintain in DCM.

$$P_{out,dcm,\max} = \frac{V_{in}^2}{27 L_L f_s} \tag{31}$$

Equation (31) becomes our first design equation. Once a switching frequency is chosen based upon the transformer design and the thermal limitations of the semiconductor

devices, the transformer leakage inductance dominates the maximum achievable power delivered to the load.

B. Converter Specifications

As described in the section above, the planned PCM-1A power converter module will provide galvanic isolation from a 1000V bus, supplying a load bank region at various levels of DC voltage. The overarching goal of the design of the converter testbed was to construct a DC-DC converter prototype for the PCM-1A standard that would be used for comparison of achievable converter power density utilizing either Si or SiC MOSFETs. To accomplish this, a single-active-bridge topology was chosen due to the findings of the study in [3], outlined in the section above. Operating points were chosen based upon a desired range of output power levels, in order to characterize the performance of the MOSFETs in the H-bridge at each point. MOSFET performance was intended to be the limiting aspect of converter operation. Thus, the transformer, filter capacitances and rectifier bridge components were derated from their maximum capabilities, so they did not limit the throughput power of the converter. Optimization of these components is outside the scope of this research.

In order to minimize switching losses within the MOSFET such that the junction temperatures of the devices increase predictably, it was chosen to maintain the converter in DCM operation for the range of operating points. Beyond the maximum power derived in Equation (31), the SAB topology enters „border“ mode operation, and the equations derived for DCM operation no longer hold. [3] A moderate switching frequency of f_s = 50 kHz was chosen to further deemphasize switching losses while remaining in a range at

which the power density of affected components is significantly high. Due to transient effects of the converter, input voltage V_{in} was chosen to be 200V to provide a safety margin while maintaining comparable converter characteristics to a device built around the PCM-1A standard, with appropriate scaling. Since transient effects of converter operation are beyond the scope of this study, the converter was designed for open-loop regulation to simplify the design of the converter control system.

Characterization of MOSFET performance corresponds to the maximum permissible power throughput of the converter, therefore regulation of the output voltage is not critical. A turns ratio of unity was selected for convenience and Equation (38) then predicts a nominal voltage of 133 V given the 200 V input voltage. The duty cycle of the converter must remain less than 2/3 in order to maintain the converter in DCM operation.

In order to construct the converter using printed circuit board (PCB) technology, a maximum DCM output power of 2 kW was chosen as the maximum rated converter power throughput. From equation (31), the required leakage inductance was found to be 14.7 μH. A summary of the converter specifications is shown in Table 5 below.

Input Voltage, V_{in}	200 V
Nominal Output Voltage, V_{out}	133 V
Maximum Power Out, P_{out}	2 kW
Nominal Duty Cycle, D_{max}	2/3
Leakage Inductance, L_l	14.7 μH

Table 5 - Converter Design Specifications

C. Transformer Design

In order to ensure that converter operation was not constrained by the electrical or thermal limitations of components other than those in the H-bridge, all magnetic, output and input filtering components were designed such that the maximum desired converter power of 2 kW was far below the maximum power throughput capabilities of the components. The transformer, specifically, was a prime component whose losses could potentially limit converter operation. A transformer design strategy was chosen that sought to minimize losses while rating the transformer for a higher maximum power than the anticipated maximum power throughput of the converter.

Leakage inductance in a transformer is classically viewed as a parasitic effect of transformer construction, which interferes with ideal assumptions about circuit operation. Transformer design strategies traditionally seek to minimize or eliminate leakage inductance effects. However, the SAB depends upon the leakage inductance for proper operation. In order to effectively control the design of the leakage inductance, a two stage approach to the design of the transformer element was chosen. First, a transformer design would be chosen which offered the least leakage inductance possible. A toroidal core was found to offer the least leakage inductance, due to the shape of the leakage field of the windings. The second stage of the design of the transformer element focused upon the addition of a series inductor with the primary winding of the transformer. The series inductance served as an effective leakage inductance whose value could be tightly controlled in the design stage.

In order to prevent converter performance from being limited by transformer losses, a power rating of 5 kVA was chosen as the maximum power throughput of the

transformer design. A Magnetics Inc. P-type core, ZP49740TC, with a relative permeability of 2500, was one most power capable toroidal cores available. This core fit within the design requirements for a low loss 5 kVA rating. Data for this core is listed in Table 6, where MLT is the effective mean-length-per-turn of the windings, A_C is the effective cross sectional area, W_A is the window area, and l_m is the mean magnetic path length.

MLT (cm)	A_C (cm^2)	W_A (cm^2)	L_m (cm)
8.21	4.223	84.3	38.15

Table 6 – Transformer Specifications

The transformer design process begins by calculating the RMS voltage applied to the primary coil of the core. If the maximum duty cycle is 2/3 by Equation (30), then the maximum RMS primary voltage is

$$V_{1,rms} = \sqrt{\frac{1}{T_s/2}\int_0^{T_{on}} V_{in}^2 dt} = 163.3V \tag{32}$$

If it is further assumed that the transformer will have to process at most 2 kVA at maximum duty cycle, then the maximum value of $V_{1,RMS}$ corresponds to an RMS primary current of 12.3 A_{RMS}. The flux linkage at this operating point is found to be

$$\lambda_1 = \int_0^{T/2_s} V_1 dt = V_{in} T_{on,\max} = V_{in} D_{\max} T_s / 2 = 1.33mVs \tag{33}$$

Given data from Magnetics, the core losses may be calculated by

$$P_{core} = K_{fe} \left(\Delta B\right)^{\beta} A_C l_M \tag{34}$$

where ΔB is the maximum swing in magnetic flux density experienced in the transformer, $\beta = 2.86$ for the P-type material used in the core and the constant K_{fe} is

$$K_{fe} = \frac{0.158 \times f_{s,kHz}^{1.36} \times 10^{2.86}}{1000} = 23.4 \tag{35}$$

The transformer design approach, developed by Erickson in [8], optimizes the core by minimizing both core and copper losses given a maximum total transformer RMS current, $I_{TOT,RMS,}$ and the converter switching frequency, f_s. The total RMS current at 2 kVA operation is then

$$I_{tot} = I_{1,rms} + \left(N_2 / N_1\right) I_{2,rms} = 24.6A \tag{36}$$

This value is used to establish the optimal transformer flux density, $\Delta\beta_{opt}$, by Equation (37), which is derived by optimizing the total transformer power losses, (sum of copper and core losses), with respect to $\Delta\beta$. Copper resistivity is assumed to be $\rho = 1.724 \times 10^{-6} \Omega cm$, and a fill factor, K_u, which defines the percentage of the window area of the transformer used for the windings, was assumed to be a reasonable value of 0.12.

$$\Delta B_{opt} = \left[\frac{10^8 \times \rho \times \lambda_1^2 \times I_{tot}^2 \times MLT}{2K_u \times W_A \times A_C^3 \times l_m \times \beta \times K_{fe}} \right]^{\left(\frac{1}{\beta+2}\right)} \tag{37}$$

Evaluating this expression gives $\Delta\beta_{opt}$ = 48 mT, which is used to derive the number of required primary turns from (38).

$$N_1 = \frac{\lambda_1 \times 10^4}{2 \times \Delta B_{opt} \times A_C} \tag{38}$$

This equation establishes that 33 turns are required on the primary and secondary sides, assuming that $N = N_1/N_2 = 1$. Given the RMS primary current value, the primary winding is needed to be equivalent to #8 AWG. In order to reduce losses due to skin and proximity effects, Litz wire from New England Wire Company, composed of interwoven small gauge wiring, was used for the winding wiring.

The equivalent leakage inductance of the transformer was incorporated by assuming that the leakage inductance of the transformer itself was negligible and adding a series inductor with the primary winding. To further minimize leakage inductance, transformer windings were interleaved, which acted to cancel leakage flux. The inductor was fabricated from a Magnetics Molypermalloy Powder (MPP) distributed air gap core (#55440). The inductor was designed for a nominal inductance of 10 μH using software provided at the Magnetics Inc. website. This resulted in the toroid being wrapped with 10 turns of #8 wire. Measurement of the total primary leakage inductance of the transformer in series with the designed inductor resulted in an inductance of 16.8 μH, measured using the primary current of the transformer during low power tests of the converter.

D. Si MOSFET Selection

The SiC transistors used in this study are 1200V and 50A DMOSFET devices. As the blocking voltage rating of a DMOSFET establishes the on-state resistance, it was necessary to choose a Si MOSFET rated at 1200V to validate comparisons between converter performance using both devices. After a survey of available components in the commercial market, the Microsemi APT26F120B2 was chosen, having a rated continuous drain current of 26A and among the best on-state resistance values available for devices rated at 1200V. Additional 600V parts were initially selected due to their extremely low on-state resistance. However, comparisons between the 600V Si devices and the 1200V SiC devices were invalid, as the lower breakdown voltage rating of the Si devices meant a decrease in on-state resistance due to decreased epitaxial layer width, not

material composition of the device. Instead, the APT26F120B2 was chosen as a comparable part to the SiC MOSFET. Pertinent operating characteristics of the device are shown below in Table 7. In order to verify the on-state resistance of the device, a Tektronix 370B curve tracer was used to establish the I-V characteristics of the MOSFET. The output of the curve tracer is shown in Figure 22.

Blocking Voltage, V_{BR} (V)	Rated On-State Current, I_{Max} (A)	Nominal On-State Resistance, $R_{DS,On}$ (Ω)	Typical Gate Charge, Q_G (nC)	Body Diode Reverse Recovery Time, t_{rr} (nS)	Thermal Junction-to-Case Resistance, $R_{\theta,J\text{-}C}$
1200	26	0.6	300	335	0.11

Table 7 - APT26F120B2 Characteristics

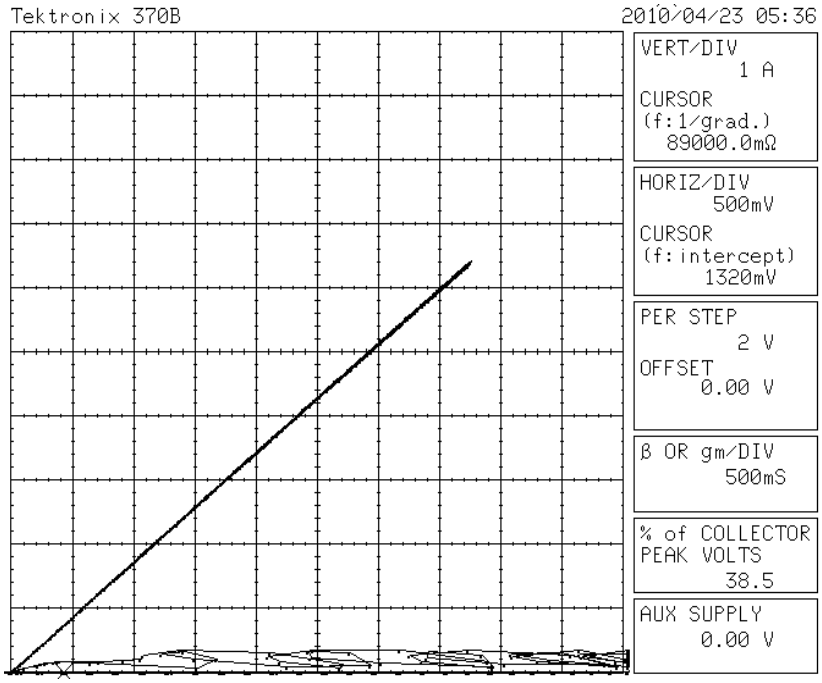

Figure 22 - APT26F120B2 Curve Tracer I-V Characteristic at 100W Maximum Throughput Power

An important characteristic of the APT26F120B2 is the variation of the on-state resistance with temperature. This variation is due to a decrease in conductivity of the

MOSFET channel with increasing temperature. Given the characteristics shown in Figure 23, losses in a power MOSFET increase with converter operating time. If the resistance of the thermal path from the junction of the device to the ambient surroundings is sufficiently high, then losses continue to increase, causing the junction temperature to destabilize. From Figure 23, $R_{DS,on}$ and consequently power losses increase by about a factor of three times the nominal on-state resistance at 100 ºC. Eventually, the junction temperature increases beyond the maximum tolerable device operating temperature, causing the MOSFET to fail. This condition is known as thermal runaway, and must be taken into account in the design of the semiconductor heatsinking apparatus.

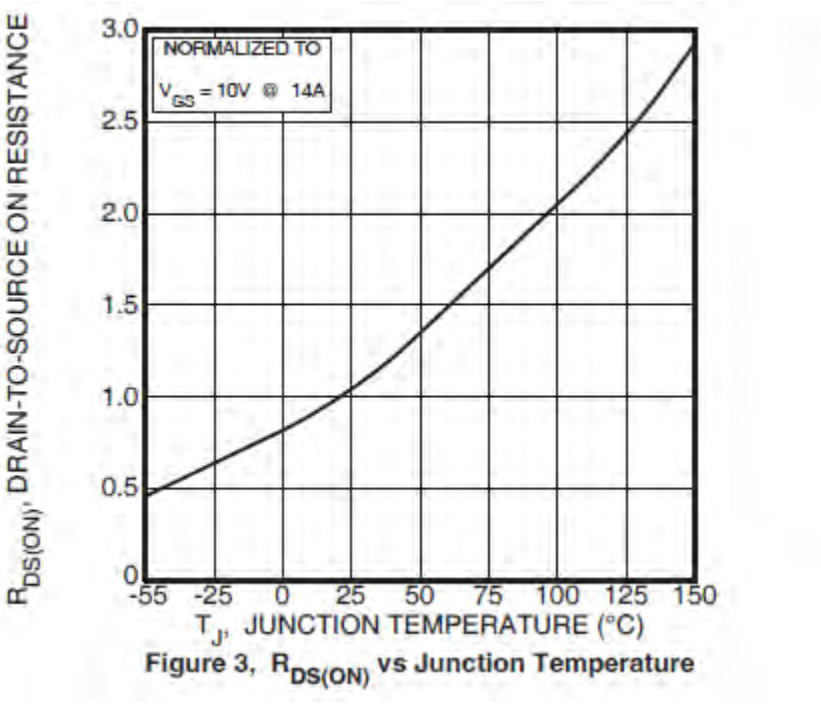

Figure 23 - APT26F120B2 On-state Resistance Temperature Characteristic

E. SiC Device Characterization

The SiC MOSFETs utilized in this study were provided by the Army Research Laboratory (ARL) in Adelphi, MD. The devices were fabricated by Cree Inc., for use in vehicular converter applications. The MOSFETs are rated for 1200V and 50A. Device characteristics were determined by measurements using a curve tracer. The I-V characteristic of the SiC FETs is shown in Figure 24.

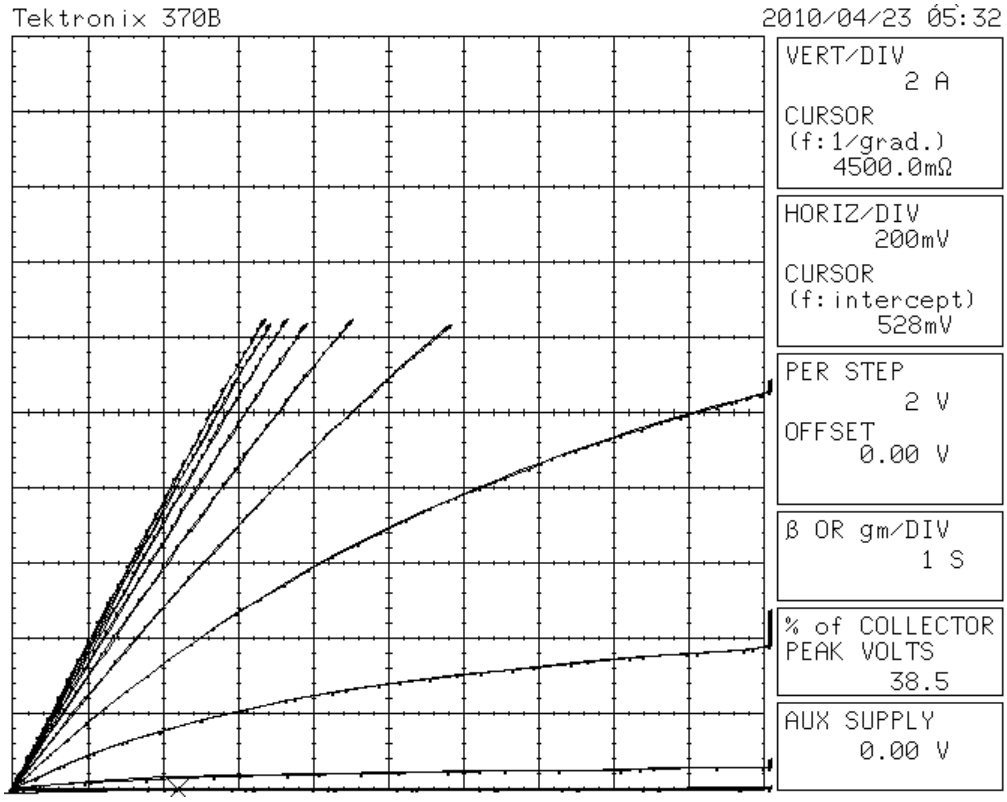

Figure 24 - 1200V SiC MOSFET Curve Tracer I-V Plot

At 15V gate voltage and room temperature, the on-state resistance of the device is 52.6 mΩ. The maximum gate voltage of the device was provided by ARL to be 20V. No significant decrease in on-state resistance is observed for gate voltages greater than 12V.

The SiC devices were provided with identically rated 1200V, 50A SiC Schottky diodes in anti-parallel with the MOSFET drain and source terminals. Schottky diodes

have negligible junction capacitance; hence, ringing losses seen due to the anti-parallel diodes in the Si MOSFETs are negligible in the SiC transistors. The devices were provided bonded onto a thermally conductive substrate. The thermal junction-to-case resistance of the device was derived from thermal performance of the device during converter operation, and was found to be 1.31 C/W.

F. Rectifier Diodes

Performance of the rectifier bridge is defined by the effective junction capacitance of the diode. Large values of junction capacitance interact with inductances in the converter circuit, causing large voltage overshoots known as ringing. Junction capacitance may be quantified by the effective diode reverse recovery time t_{rr}, the time required to remove charge stored in the diode during on-state operation. [15] IXYS DSEI60-06 Fast Recovery Diodes (FREDs), with a blocking voltage of 600V and a continuous current rating of 60A, were chosen. The t_{rr} of this diode is 50 ns. The characteristics of the DSEI60-06A are listed in Table 8.

Blocking Voltage, V_{BR} [V]	Maximum Rated Current, I_{Max} [A]	Reverse Recovery Time, t_{rr} [ns]	Thermal Junction-to Case Resistance, $R_{\theta,JC}$ [C/W]
600	60	50	0.29

Table 8 - 1200V SiC MOSFET Characteristics

G. Semiconductor Heatsinking

Junction temperature of a semiconductor device is strongly affected by the thermal path through which heat generated by power losses is removed from the device. As demonstrated in the background section above, volume of the heatsinking apparatus

must increase to maintain the junction temperature below the maximum permissible device operating temperature. If the thermal resistance of the heatsinking apparatus becomes higher than the optimal value for a given semiconductor power loss, the junction temperature will rise beyond the value provided by the optimal heatsink. For devices such as MOSFETs, thermal cooling pathways must be carefully designed to avoid thermal runaway.

If the heatsinking apparatus is not designed to limit T_s for the anticipated converter throughput power, the junction temperature becomes the limiting factor in converter operation. Hence, the maximum converter throughput power is defined by the operating point at which the maximum allowable junction temperature is reached. This strategy allows for direct judgment of converter performance utilizing different semiconductor technology.

In order to establish a worst-case limit for performance of the topology, the heatsinking apparatus is not chosen to be optimal for the maximum allowable MOSFET junction temperature. Instead, commercially bought heatsinks are chosen with a reasonable thermal resistance for the expected losses. For both the inverter H-bridge and the rectifier bridge, an Aavid Thermalloy HS380-ND heatsink was chosen, shown below in Figure 25. Using forced-air convection, the thermal resistance of the heatsink varies according to the curve shown in Figure 26.

Figure 25 - HS380 Heatsink

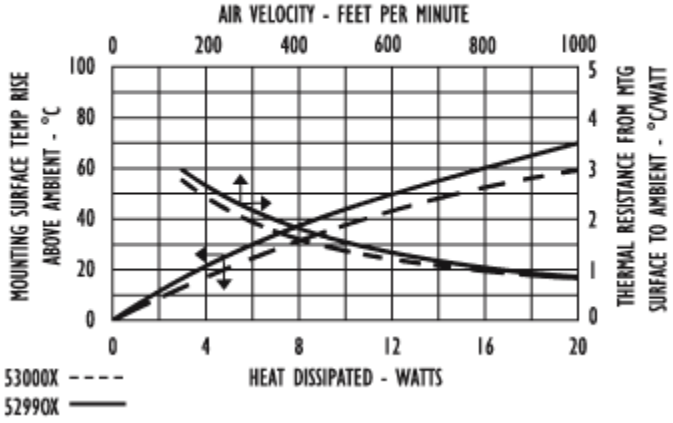

Figure 26 - HS380 Thermal Resistance Characteristics versus Flow Rate

To provide forced-air convection across the heat sinks, three Sunon SP100A fans were chosen. The SP100A is single speed induction motor fan, capable of 115 cubic feet per minute (CFM) with a face area of 14,400 mm^2, corresponding to an air velocity of 741.93 ft/minute. Utilizing these fans, the effective thermal resistance of the HS380-ND is 1.1 °C/W.

In order to eliminate air pockets between the semiconductor device casing and the heat sink, thermal compounds were applied to the MOSFET-heat sink interface. For the Si APT26F120B2, MG Chemicals TC-450ML thermal epoxy was used to connect the device both thermally and mechanically to the heat sink. The thermal resistance of the interface layer was calculated using the thermal conductivity of the material and the width and area of the layer. The estimated thermal resistance of the TC-450ML layer was 0.11 ºC/W. For the SiC MOSFETs, Arctic Silver thermal grease was utilized. The estimated thermal resistance of this material was 0.17 ºC/W.

H. Converter Control

In order to generate the gating scheme laid out in the analysis of the operation of the SAB converter in Section A, an Altera Cyclone II field programmed gate array (FPGA) on an Altera DE2 Development and Education board was programmed to generate the necessary logic signals to control MOSFET switching. The gating program was written in the VHDL hardware programming language, using a timer routine to control frequency and pulse-width modulation of the phase-shifted half-bridge. The gating code may be found in Appendix A. Duty cycle adjustment was input as a binary input using an array of DIP switches. A preset ramp-up time of five seconds to the input duty cycle was programmed into the board in order to mitigate transients at start up of the converter.

To gate a MOSFET into conduction, sizeable gate currents must be sourced and sunk to provide the charge necessary to create a conduction channel within the device. A

driver interface chip must be used to accomplish this requirement. In a bridge circuit, a „boot-strap" circuit must be used on the high side MOSFETs because the voltage on the gates of these devices must be greater than the source connection. The International Rectifier IRS2186 high and low-side driver was chosen for this purpose. The chip is CMOS logic compatible with 4A of sourcing and sinking current capability and has propagation delays of no more than 250 ns. A 0.1 μF capacitor was used as a bootstrap capacitor for the high-side switch. A 15V driver voltage was used, and a 15 Ω resistor coupled the driver to the FETs to limit the current supplied by the chip.

I. Input and Output Capacitances

In steady-state operation, average capacitor charge at the input and output must be equal to zero. Thus, we can use the input and output ripple current to derive the required capacitances. Taking the integral of the ripple current of the input and output current waveforms, the capacitances can be derived by Equation (39). In (39), Δi_C is the ripple current across the capacitor, and ΔV_o is the desired maximum output voltage ripple.

$$C_f = \frac{\Delta i_C}{8 \Delta V_o f_s} \tag{39}$$

Instead of the original switching frequency of 50 kHz, it must be noted that the effective frequency of the rectified current $i_{Rect,out}$ shown in Figure 21 above is doubled to 100 kHz by the effects of rectification. The same effect is noted in the input current waveform.

Using Equation (39), input and output filter capacitors were chosen. Both were chosen to tolerate a minimum blocking voltage of 450V, handle a ripple current of 30A and exhibit minimal equivalent series inductance (ESL). An EPCOS B3454A5 capacitor

with a value of 1000 μF was chosen as the input capacitance, rated for 450V and 22A of ripple current capability. For the output, an AVX FFVE6K0107K 100 μF capacitor was chosen, rated for 600V and 130A of ripple current. Characteristics of the input and output capacitors are shown below in Table 9.

	Capacitance	*Voltage Rating* [V]	*Ripple Current Capability* [A]
EPCOS B3454A5	1000 μF	450	22
AVX FFVE6K0107K	100 μF	600	130

Table 9 – Filter Capacitor Characteristics

J. Converter Construction and Effective Volume

A completed converter is shown in Figure 27. Due to the size of the transformer, it was decided to divide the circuit into five sections: input capacitor, H-bridge, transformer, output rectifier, and output capacitor. Separate printed circuit boards are used for the H-bridge inverter and the rectifier bridge. The transformer, input and output capacitors are placed between. Three SP100 fans were placed behind the converter. The layout of the converter gives a direct thermal airflow path across every component.

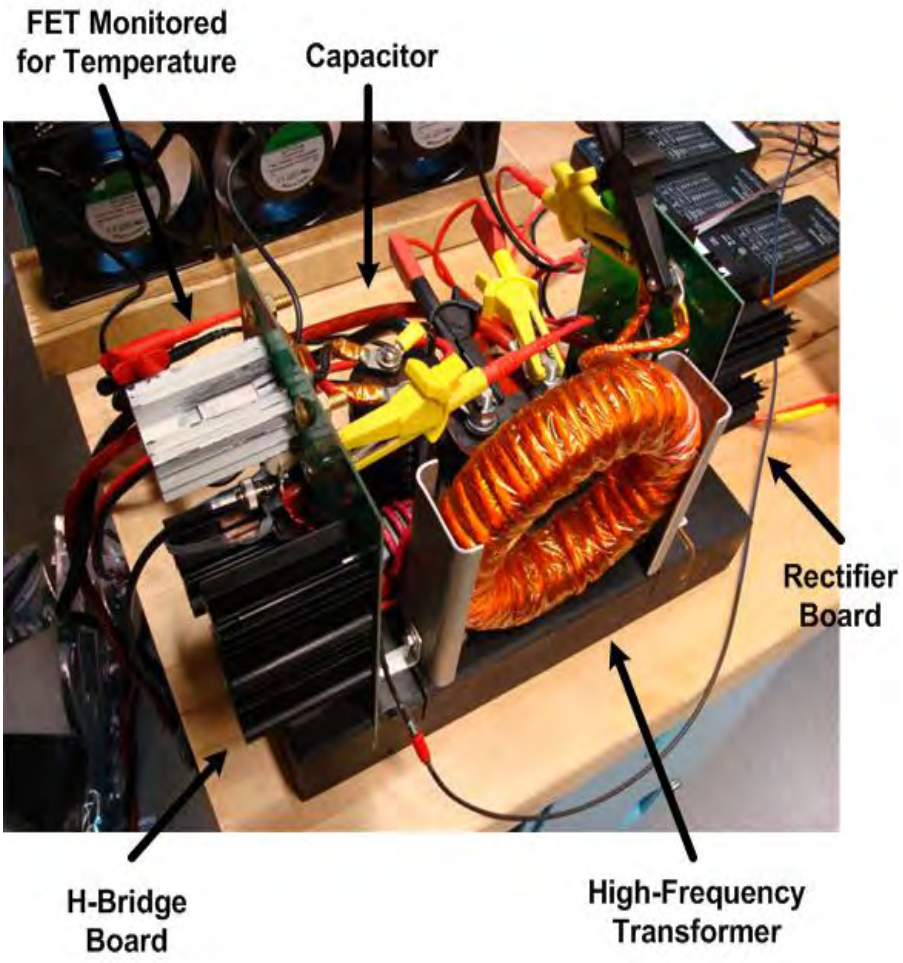

Figure 27 - Completed SAB Testbed Converter

To characterize converter power density, effective converter volume was needed. Volume of the converter base, printed circuit boards, semiconductor packaging and control circuitry are small enough to be considered negligible. The volume of the converter is taken to be the sum of the heatsinking volume, transformer and inductor cores volumes, and filter capacitance volumes. The volumetric distribution of the converter is shown in Table 10. The effective converter volume was found to be 1168.513 cm^3. It is important to re-emphasize that this is not an optimized volume for the given power throughput rating.

Semiconductor Heatsink	Aavid Thermalloy HS380-ND	540.776 cm^3
Transformer Core	Magnetics Inc. ZP49740TC	161.086 cm^3
Input Capacitance	EPCOS B43564	221.036 cm^3
Output Capacitance	AVX FFVE6K0107K	224.318 cm^3
Primary Inductor	Magnetics 55440	21.300 cm^3
	Effective Converter Volume	1168.513 cm^3

Table 10 - Volume of Key Converter Components

K. Converter Testbed Setup

The testing setup, shown in block diagram form in Figure 28, uses a Sorenson SGA 600V/17A high-power programmable DC power supply as the input to the converter. An Avtron Spirit load bank rated for 800V and up to 62.5A was used as the load. Settings on the load bank allow for a 5A resolution in maximum tolerable current between load steps. A FLIR A320 infrared camera monitored semiconductor device temperatures and also surface temperatures of other components such as the transformer and gate drivers. A Tektronix 5104B 4-channel, 1GHz oscilloscope was used to observe and store various circuit waveforms. A PEM CWT ULTRA mini Rogowski coil with a 20MHz bandwidth was employed to measure the transformer primary current. Tektronix P5200 voltage isolators measured the drain-to-source voltage of the low-side leading FET and the transformer primary and secondary voltages.

Complete Testbed Layout

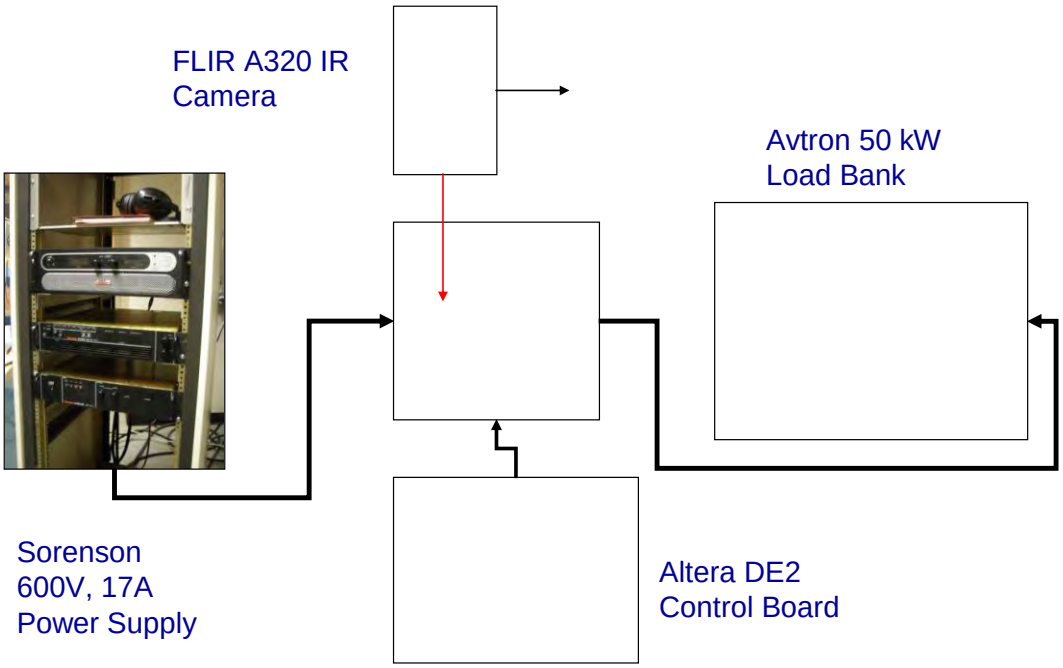

Figure 28 - Laboratory Testbed System Setup

V. Results of Converter Testing

Two SAB converters utilizing Si and SiC MOSFET technologies in the inverter bridge were successfully built and operated under various load conditions. At each operating point, junction temperature was measured directly and indirectly using the IR camera. Original testing procedures called for power density to be determined by the power throughput level at which the MOSFET junction temperature reached 100 ºC. Power density was thus judged at the maximum achieved steady-state junction temperature common to all converters. Comparison of this metric allows for definitive conclusions to be drawn on the benefits of using SiC MOSFETs to improve converter power density and overall converter performance.

A. Deviations from Ideal Converter Operation

In the previous analysis of the electrical characteristics of the SAB circuit, components such as diodes were assumed to be ideal and lossless. However, actual diodes possess junction capacitances which interact with inductive circuit elements to create oscillations known as „ringing". Ringing causes additional switching losses in semiconductor devices, and cause waveform trajectories to deviate from those derived in the ideal case.

The effects of ringing are most significant due to the interaction between the junction capacitances of the rectifier bridge and the leakage inductance of the transformer. These oscillations have a measured resonant frequency of approximately 1 MHz, and occur at turn off of the rectifier diodes due to the primary current reaching zero before the end of the half period. Secondary-side ringing is clearly shown in the oscilloscope capture of Figure 29.

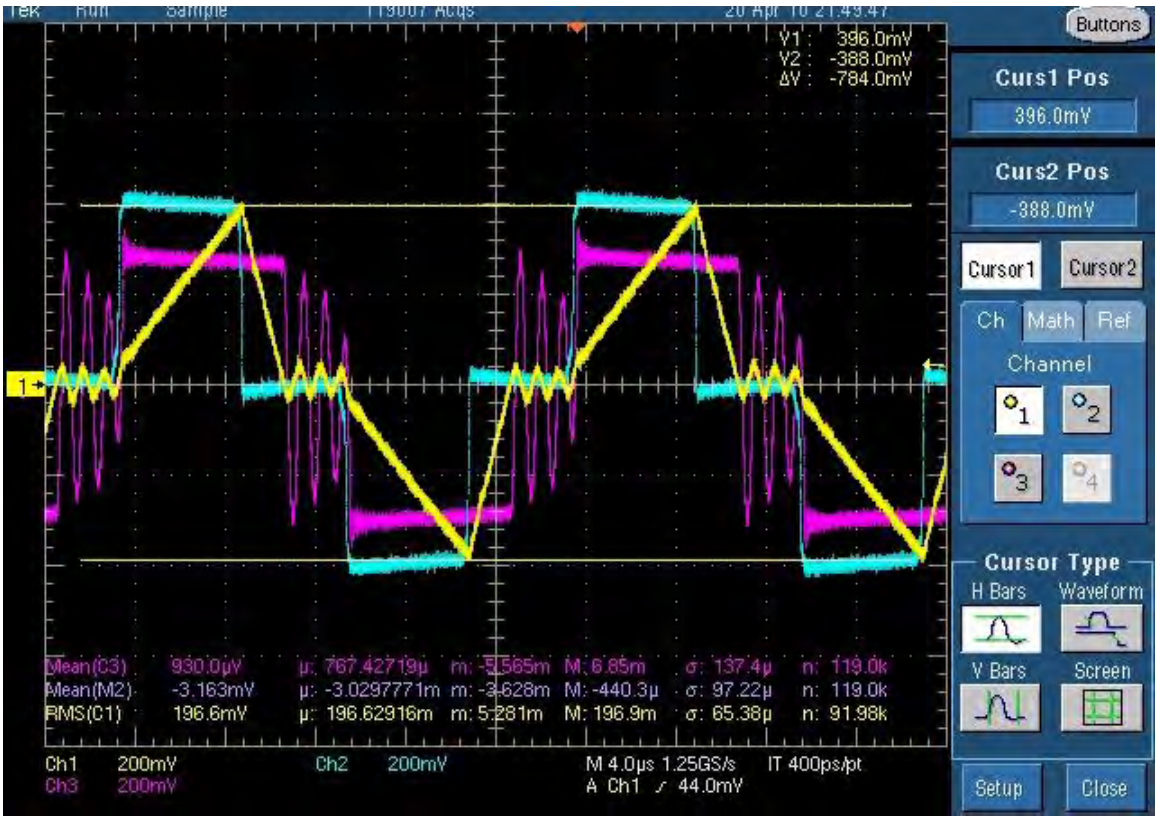

Figure 29 - Primary and Secondary Voltages and Primary Current

Though ringing was significant in the secondary-side voltage, overall predicted converter operation was not appreciably affected. The waveforms of Figure 29 correspond to an input voltage of 200 V, an effective duty cycle of 56 percent and an output resistance of 18.8 Ω. For these values, Equation (22) predicts a peak primary current i_{pk} of 19.6 A. The actual measured value i_{pk} was 19.8 A, within one percent of the predicted value.

B. Converter Power Density using APT26F120B2 MOSFETs

Initial tests were carried out using Si APT26F120B2 MOSFETs in the inverter bridge. A duty cycle of 9.89 percent was chosen and kept constant throughout the test range. Power output was stepped by progressively decreasing the load resistance by equal $1/R_{out}$ amounts. Junction temperature was found by measuring the heat sink temperature using thermography and employing the thermal model of the heatsink to estimate the junction temperature. System efficiency was measured by monitoring DC input and output current and voltage levels using Tektronix A622 Hall-effect current probes and P5210 differential voltage isolators. Results of testing are shown in Table 11. Heatsink and junction temperature are plotted against output power in Figure 30 for datapoints which displayed thermal stability.

Rout (Ω)	Vout (V)	Pin (W)	Pout (W)	T_j (C)	Eff (%)	Thermal Runaway
45.7	131.82	346	262.3218	68.6688	75.82	
35.6	117.83	388.0388	295.7533	72.576	76.22	
29.1	110.67	430	340.8636	76.72	79.27	
24.6	90.47	510.1275	379.974	78.0224	74.49	
21.3	89.01	588.2646	372.9519	89.744	63.40	> 15 Minutes

Table 11 - Converter Performance Data using APT26F120B2 MOSFETs

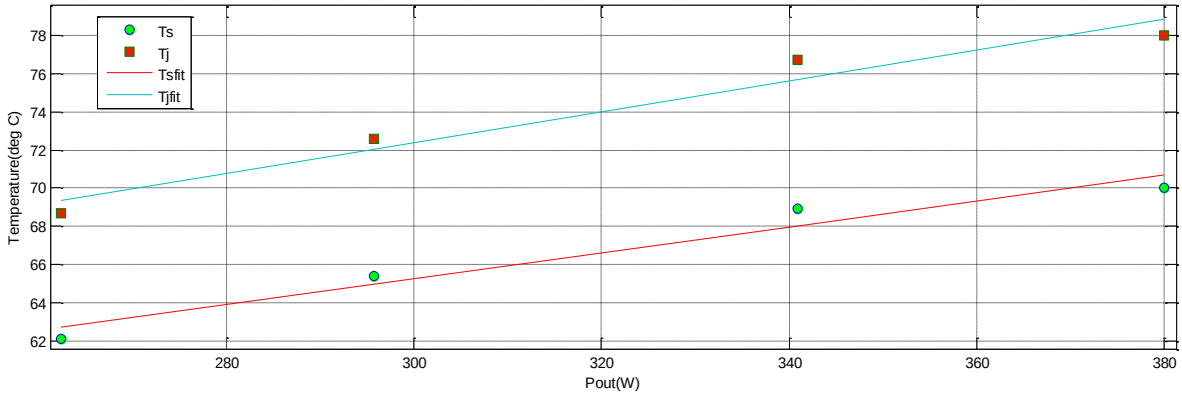

Figure 30 - Thermally Stable Si Junction and Heatsink Temperatures versus Output Power

Due to the temperature characteristic of the on-state resistance value of the APT26F120B devices, junction temperatures failed to stabilize past an output power of 379.9 W, at a load resistance of 24.6 Ω, going into a state of thermal runaway. An IR screenshot of the device under test is shown in Figure 31 at 379.9W output power, after 5 minutes of operation. At a load resistance of 21.33 Ω, corresponding to an input power of 588.26 W, converter efficiency fell dramatically to 63.4 percent. Device junction temperature stabilized briefly at 89.7 ºC at 15 minutes of testing before thermally destabilizing. The decreased efficiency of the converter at higher loss levels corresponds with the expected rise in MOSFET on-state resistance with junction temperature. This rise also accounts for the noted non-linearity of temperature increase.

Figure 31 - Si Device IR Screenshot after 5 minutes of operation; $T_{sink,f}$ = 70.5 ºC

Two values of power density can be derived from the results of testing with the APT26F120B2 devices. A maximum output power of 379.95 W was measured at which the junction temperature reached thermal stability. The junction temperature reached 78.02 ºC at this power throughput point. Using this value as the maximum throughput power and the converter volume found in the previous section, the converter demonstrates an approximate power density of 0.325 MW/m^3. If thermal limitations are neglected, a linear extrapolation can be fit to the data to recover the potential throughput power at which a junction temperature of 100 ºC is reached. Using this best-fit line, which is plotted on Figure 30, a power density of 0.550 MW/m^3 is estimated. Both of these measurements can be compared to the performance of the converter utilizing SiC devices to draw conclusions.

C. Converter Power Density using SiC MOSFETs

Following testing using Si MOSFETs, the H-bridge inverter section of the converter was replaced by an identical inverter using SiC devices. Since testing revealed that thermal runaway was not apparent over the converter output power range, a larger duty cycle of 47.17 percent was chosen to offer larger steps in output power per step in load resistance. Junction temperature and system efficiency were monitored using identical methods as in the previous dataset using Si devices. Results are shown in Table 12 and graphed in Figure 33. Data was recorded until the junction temperature surpassed 100 ºC.

Rout (Ω)	Vout (V)	Pin (W)	Pout (W)	T_j (C)	Eff (%)
64	176.0	542	519	40.7	95.8
45.7	168.5	694	664	48.1	95.7
35.6	158.9	800	757	56	94.6
29.1	152.6	910	856	62.7	94.0
24.6	150.2	1042	979	70.7	94.0
21.3	147.0	1154	1079	76.9	93.5
18.8	141.1	1224	1127	83.2	92.1
16.8	135.1	1262	1156	90.9	91.6
15.2	132.1	1346	1221	96.9	90.7
13.9	131.5	1457	1328	101.8	91.1
12.8	129.3	1534	1384	107.1	90.2

Table 12 - Converter Performance Data using SiC MOSFETs

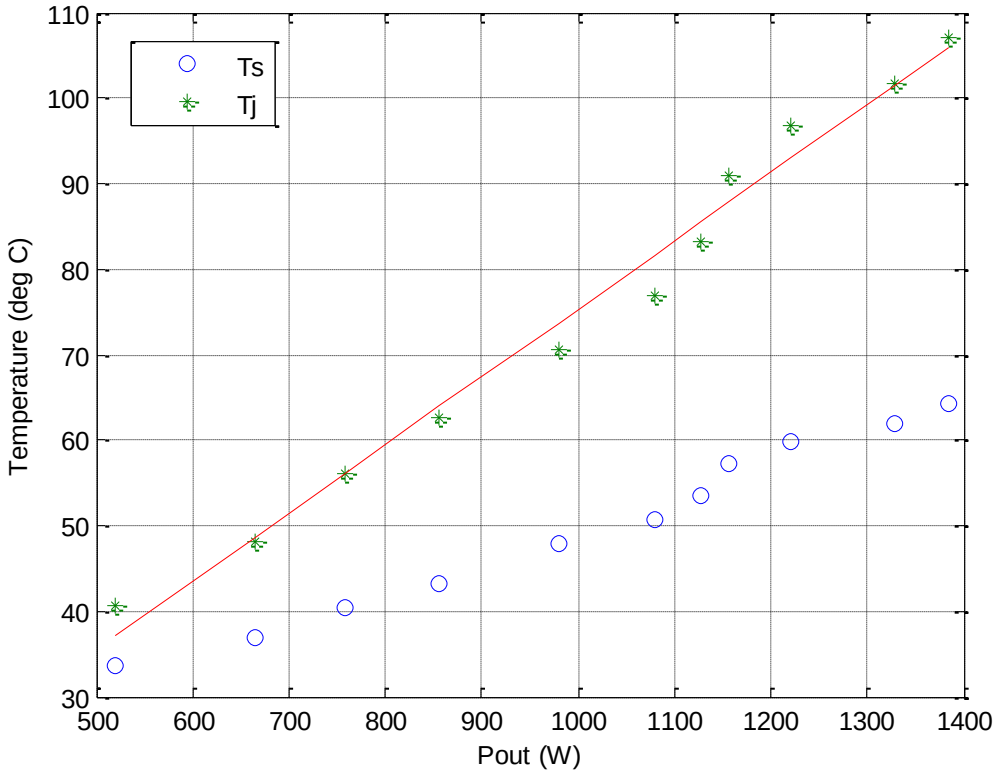

Figure 32 – SiC MOSFET Junction and Heatsink Temperatures versus Output Power

As expected, in the absence of thermal runaway junction temperature of the MOSFETs increases linearly. An IR screenshot of the device under test at a maximum converter output power of 1384 W is shown in Figure 34. This is the maximum output power attainable given the minimum load resistance of 12.8 Ω. A least squares regression was fit to the data to estimate the output power at which the junction temperature of the devices reached 100 ºC. Using the linear fit, the output power was found to be 1206.4 W at this operating point. This output power level corresponds to a power density of 1.032 MW/m^3. For comparison to the first power density figure found from the Si converter, output power at 78.02 ºC was 929.92 W, corresponding to a power density of 0.796 MW/m^3.

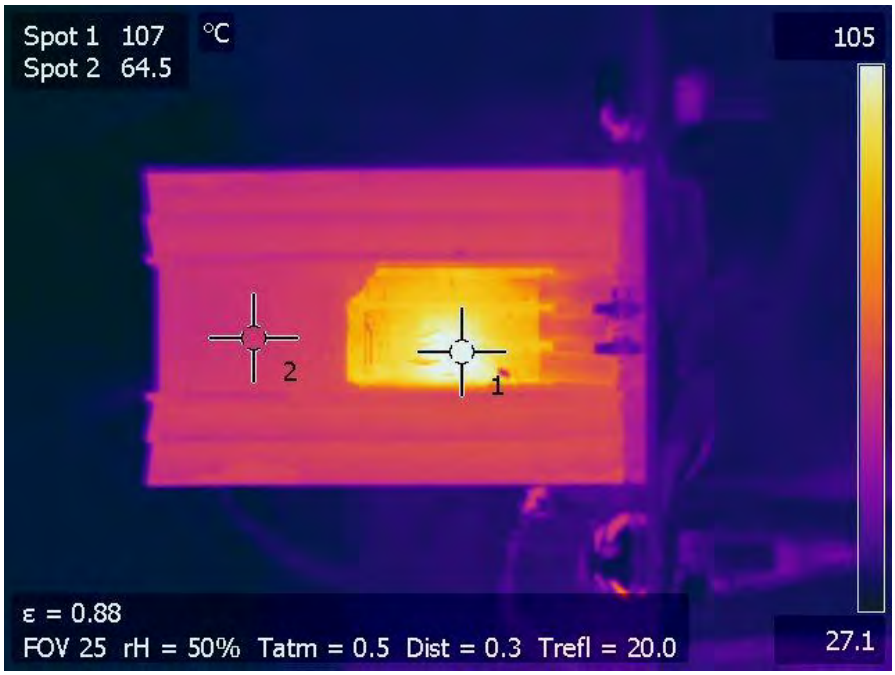

Figure 33 - SiC Device IR Screenshot at Maximum Throughput Power; $T_{j,f}$ = 107 ºC

D. Comparison of Si versus SiC Power Density Figures

Due to thermal runaway, device junction temperatures could not be realistically compared at the nominal junction temperature of 100 ºC. However, power density performance comparisons can still be made between the two converters by adjusting the maximum allowable junction temperature to the maximum junction temperature achieved by the Si devices. Power density figures found using a maximum junction temperature of 78.02 ºC are shown in Table 13 below.

	ρ, T_j = 78.02 ºC	ρ, T_j = 100 ºC
Si APT26F120B2	0.325 MW/m3	0.550 MW/m3
SiC MOSFETs	0.795 MW/m3	1.02 MW/m3

Table 13 - Power Density Figures for Si and SiC Enabled Converters

Using a best-fit line and disregarding thermal runaway effects, results from tests using the APT26F120B2 devices can be extended to a hypothetical point at which junction temperatures reach 100 ºC. This method gives a higher power density figure than the measured value achieved prior to thermal runaway. The power density figures for a junction temperature of 100 ºC are shown in the rightmost column of Table 13.

Comparison of the power density figures demonstrates the capabilities of SiC devices to increase of power density within a given converter design. For a maximum junction temperature of 78.02 ºC, a 244.6 percent increase in power density is observed between the Si and SiC enabled converters. For a junction temperature of 100 ºC, a 185.5 percent increase is seen. Though the power density of the SiC converter falls short of reaching a power density of 3 MW/m^3 set out by ONR, an optimized design using SiC devices could surpass this goal. Further study is needed to determine the level at which converter optimization affects converter power density, and is outside the scope of this study.

VI. Conclusions

This project successfully demonstrated that the use of SiC MOSFETs in a SSCM prototype offers a significant increase in converter power density over similarly rate Si MOSFET devices, and offers a method of increasing shipboard converter power density to levels desired for future electric ship IPS architectures. A method of directly comparing power density figures between converters employing both Si and SiC MOSFETs was explored. By using a thermographic method, non-intrusive measurements of device junction temperature can be measured and used to characterize converter performance. To facilitate this comparison, a candidate SSCM prototype was designed and built as a testbed for device comparison. Using a single active bridge topology, power density of the converter was found to increase by 244.6 percent given a maximum allowable junction temperature of 78.02 C using SiC devices. Improvements in power density were further demonstrated by extrapolating results beyond the thermal limitations of the Si devices. At a maximum junction temperature of 100 ºC, SiC devices demonstrate a 185.5 percent improvement in converter power density. These figures can be used by future designers to judge improvements offered by the use of SiC MOSFETs in an SSCM design.

To successfully implement the NGIPS in volumetrically constrained platforms such as small surface combatants and submarines, bus converter modules must be made optimally power dense in order to decrease volumetric requirements of the modules for a rated throughput power. Though the converters in the project are sub-optimal, optimally designed power converters with SiC devices should offer significant savings in volume in shipboard power distribution systems. Using SiC, the Navy will be able to increase the

power density of shipboard power converter modules to levels required for successful implementation of the MVDC IPS architecture.

VII. Suggestions for Further Work

A significant amount of follow-on work is motivated by these investigations. First, data must be recollected for the Si-parts with the parts properly de-encapsulated so that a direct junction temperature measurement can be made and the indirect method accuracy better assessed. Second, despite being able to measure power density for the thermal constraint imposed, effort must next be applied to achieving an overall "optimized" converter design, where the switching frequency, transformer, rectifier output, and cooling system are considered in more detail. This will entail a more detailed consideration of "ringing losses" as well as different transformer core shapes and materials. Third, devices using breakdown voltages closer to the rated voltage of the converter could be used, or converter input and output voltage levels raised to levels comparable to 1200V. Additionally, further work on the output rectifier snubber is necessary to reduce the ringing in the voltage on the secondary-side of the transformer. Finally, theoretical studies are required to compare the power density performance of the active bridge in the discontinuous conduction mode versus operation in what is referred to as the "boundary mode." This would allow the designer to better understand the tradeoffs between switching losses and conduction losses as higher frequencies are considered.

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Appendix A: Converter Controller VHDL Coding

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
use ieee.std_logic_unsigned.all;

entity fullbridgePWMcontrol is

port (
    -- Clocks

    CLOCK_27,                                       -- 27 MHz
    CLOCK_50,                                       -- 50 MHz
    EXT_CLOCK : in std_logic;                       -- External Clock

    -- Buttons and switches

    KEY : in std_logic_vector(3 downto 0);          -- Push buttons
    SW : in std_logic_vector(17 downto 0);          -- DPDT switches

    -- LED displays

    HEX0,  HEX1,  HEX2,  HEX3,  HEX4,  HEX5,  HEX6,  HEX7  --  7-segment
displays
       : out std_logic_vector(6 downto 0);
    LEDG : out std_logic_vector(8 downto 0);        -- Green LEDs
    LEDR : out std_logic_vector(17 downto 0);       -- Red LEDs

    -- RS-232 interface

    UART_TXD : out std_logic;                       -- UART transmitter
    UART_RXD : in std_logic;                        -- UART receiver

    -- IRDA interface

    IRDA_TXD : out std_logic;                       -- IRDA Transmitter
    IRDA_RXD : in std_logic;                        -- IRDA Receiver

    -- SDRAM

    DRAM_DQ : inout std_logic_vector(15 downto 0); -- Data Bus
    DRAM_ADDR : out std_logic_vector(11 downto 0); -- Address Bus
    DRAM_LDQM,                                        -- Low-byte Data
Mask
    DRAM_UDQM,                                       -- High-byte Data
Mask
    DRAM_WE_N,                                      -- Write Enable
    DRAM_CAS_N,                                      -- Column Address
Strobe
    DRAM_RAS_N,                                         -- Row Address
Strobe
    DRAM_CS_N,                                      -- Chip Select
    DRAM_BA_0,                                      -- Bank Address 0
    DRAM_BA_1,                                      -- Bank Address 0
    DRAM_CLK,                                       -- Clock
```

```
    DRAM_CKE : out std_logic;                       -- Clock Enable

    -- FLASH

    FL_DQ : inout std_logic_vector(7 downto 0);      -- Data bus
    FL_ADDR : out std_logic_vector(21 downto 0);  -- Address bus
    FL_WE_N,                                          -- Write Enable
    FL_RST_N,                                         -- Reset
    FL_OE_N,                                          -- Output Enable
    FL_CE_N : out std_logic;                          -- Chip Enable

    -- SRAM

    SRAM_DQ : inout std_logic_vector(15 downto 0); -- Data bus 16 Bits
    SRAM_ADDR : out std_logic_vector(17 downto 0);  -- Address bus 18
Bits
    SRAM_UB_N,                                          -- High-byte Data
Mask
    SRAM_LB_N,                                           -- Low-byte Data
Mask
    SRAM_WE_N,                                        -- Write Enable
    SRAM_CE_N,                                        -- Chip Enable
    SRAM_OE_N : out std_logic;                        -- Output Enable

    -- USB controller

    OTG_DATA : inout std_logic_vector(15 downto 0); -- Data bus
    OTG_ADDR : out std_logic_vector(1 downto 0);    -- Address
    OTG_CS_N,                                         -- Chip Select
    OTG_RD_N,                                         -- Write
    OTG_WR_N,                                         -- Read
    OTG_RST_N,                                        -- Reset
    OTG_FSPEED,                        -- USB Full Speed, 0 = Enable, Z =
Disable
    OTG_LSPEED : out std_logic;      -- USB Low Speed, 0 = Enable, Z =
Disable
    OTG_INT0,                                           -- Interrupt 0
    OTG_INT1,                                           -- Interrupt 1
    OTG_DREQ0,                                          -- DMA Request 0
    OTG_DREQ1 : in std_logic;                           -- DMA Request 1
    OTG_DACK0_N,                                          -- DMA Acknowledge
0
    OTG_DACK1_N : out std_logic;                        -- DMA Acknowledge
1

    -- 16 X 2 LCD Module

    LCD_ON,                     -- Power ON/OFF
    LCD_BLON,                   -- Back Light ON/OFF
    LCD_RW,                        -- Read/Write Select, 0 = Write, 1 =
Read
    LCD_EN,                     -- Enable
    LCD_RS : out std_logic;      -- Command/Data Select, 0 = Command, 1
= Data
    LCD_DATA : inout std_logic_vector(7 downto 0); -- Data bus 8 bits

    -- SD card interface
```

```
    SD_DAT,                     -- SD Card Data
    SD_DAT3,                    -- SD Card Data 3
    SD_CMD : inout std_logic;   -- SD Card Command Signal
    SD_CLK : out std_logic;     -- SD Card Clock

    -- USB JTAG link

    TDI,                        -- CPLD -> FPGA (data in)
    TCK,                        -- CPLD -> FPGA (clk)
    TCS : in std_logic;         -- CPLD -> FPGA (CS)
    TDO : out std_logic;        -- FPGA -> CPLD (data out)

    -- I2C bus

    I2C_SDAT : inout std_logic; -- I2C Data
    I2C_SCLK : out std_logic;   -- I2C Clock

    -- PS/2 port

    PS2_DAT,                    -- Data
    PS2_CLK : in std_logic;     -- Clock

    -- VGA output

    VGA_CLK,                                            -- Clock
    VGA_HS,                                             -- H_SYNC
    VGA_VS,                                             -- V_SYNC
    VGA_BLANK,                                          -- BLANK
    VGA_SYNC : out std_logic;                           -- SYNC
    VGA_R,                                              -- Red[9:0]
    VGA_G,                                              -- Green[9:0]
    VGA_B : out std_logic_vector(9 downto 0);           -- Blue[9:0]

    --  Ethernet Interface

    ENET_DATA : inout std_logic_vector(15 downto 0);      -- DATA bus
16Bits
    ENET_CMD,           -- Command/Data Select, 0 = Command, 1 = Data
    ENET_CS_N,                                          -- Chip Select
    ENET_WR_N,                                          -- Write
    ENET_RD_N,                                          -- Read
    ENET_RST_N,                                         -- Reset
    ENET_CLK : out std_logic;                           -- Clock 25 MHz
    ENET_INT : in std_logic;                            -- Interrupt

    -- Audio CODEC

    AUD_ADCLRCK : inout std_logic;                      -- ADC LR Clock
    AUD_ADCDAT : in std_logic;                          -- ADC Data
    AUD_DACLRCK : inout std_logic;                      -- DAC LR Clock
    AUD_DACDAT : out std_logic;                         -- DAC Data
    AUD_BCLK : inout std_logic;                            -- Bit-Stream
Clock
    AUD_XCK : out std_logic;                            -- Chip Clock

    -- Video Decoder
```

```
    TD_DATA : in std_logic_vector(7 downto 0);  -- Data bus 8 bits
    TD_HS,                                      -- H_SYNC
    TD_VS : in std_logic;                       -- V_SYNC
    TD_RESET : out std_logic;                   -- Reset

    -- General-purpose I/O

    GPIO_0, -- GPIO Connection 1
    GPIO_1: out std_logic_vector(35 downto 0)
    );
end fullbridgePWMcontrol;

architecture arch_PWM of fullbridgePWMcontrol is

signal reg_out : std_logic_vector( 8 downto 0 );
signal    cnt_out_int,    cnt_out_int2,    cnt_out_int3,    cnt_out_int4:
std_logic_vector(8 downto 0);
signal pwm_int, rco_int, pwm_int2, rco_int2,
      pwm_int3, rco_int3, pwm_int4, rco_int4: std_logic;
signal pwm2_en, pwm4_en: std_logic;
signal  fullperiod1,  fullperiod2,  fullperiod3,  fullperiod4  :  integer
range 0 to 2;
signal startup_en : std_logic;
signal startup : std_logic_vector( 8 downto 0 );
signal ramp_up : integer range 0 to 999999;
signal enabe : std_logic;

begin

enabe <= SW(17);    -- Rightmost

pwm_control: process( fullperiod1, fullperiod2, enabe  )
begin
      if( enabe = '0' ) then
            pwm2_en <= '0';
      end if;

      if(fullperiod1 = 2) then
            pwm2_en <= '1';
      end if;

      if(fullperiod2 = 2) then
            pwm2_en <= '0';
      end if;
end process;

startup_counter: process( CLOCK_50, enabe, SW(8 downto 0),
      startup_en, startup )
begin
      if( enabe = '0' ) then
            startup_en <= '1';
            startup <= "000000000";
            ramp_up <= 0;
      elsif( rising_edge(CLOCK_50) and startup_en = '1') then
            ramp_up <= ramp_up + 1;
            if( ramp_up = 999999 ) then
```

```
                  startup <= startup + "000000001";
                  if( startup < SW(8 downto 0) ) then
                        startup_en <= '1';
                  elsif( startup = SW(8 downto 0) ) then
                        startup_en <= '0';
                  end if;
                  ramp_up <= 0;
            end if;
      end if;
end process;

data_register: process( CLOCK_50, reg_out, SW(8 downto 0),
      enabe )
begin
      if( enabe = '0'  ) then
            reg_out <= "000000000";
      elsif( rising_edge(CLOCK_50) ) then
            if( startup_en = '1' ) then
                  reg_out <= startup;
                  HEX7     <= "0010010"; -- S(tate)
                  HEX6     <= "1111001"; -- 1
                  HEX5     <= "1000000"; -- 0
                  HEX4     <= "0010010"; -- 5
                  HEX3     <= "0010010"; -- S
                  HEX2     <= "0000110"; -- E
                  HEX1     <= "1000110"; -- C
                  HEX0     <= (others => '1');
            elsif( startup_en = '0' ) then
                  reg_out <= SW(8 downto 0);
                  HEX7     <= "0010010"; -- S
                  HEX6     <= "0100100"; -- 2
                  HEX3     <= "0001100"; -- P
                  HEX2     <= "1000110"; -- C
                  HEX1     <= "0000111"; -- T
                  HEX0     <= (others => '1');


                  if( SW(8 downto 0) = "011111010" ) then --50%
                        HEX5 <= "0010010";
                        HEX4 <= "1000000";
                  elsif( SW(8 downto 0) = "111110011" ) then --99%
                        HEX5 <= "0010000";
                        HEX4 <= "0010000";
                  elsif( SW(8 downto 0) = "000000001" ) then -- 1%
                        HEX5 <= "1000000";
                        HEX4 <= "1111001";
                  elsif( SW(8 downto 0) >= "101110111" ) then     --
>375, 75%
                        HEX5 <= "1111000";
                        HEX4 <= "0010010";
                  elsif( SW(8 downto 0) > "011111010" and SW(8 downto
0) < "101110111"  ) then -- >250 67%
                        HEX5 <= "0000010";
                        HEX4 <= "1111000";
                  elsif( SW(8 downto 0) > "001111101" and SW(8 downto
0) < "011111010" ) then -- >125 37%
                        HEX5 <= "0110000";
```

```
                        HEX4 <= "1111000";
                  elsif( SW(8 downto 0) = "001111101" ) then      --
125 25%
                        HEX5 <= "0100100";
                        HEX4 <= "0010010";
                  elsif( SW(8 downto 0) < "001111101" ) then      --
<125 12%
                        HEX5 <= "1111001";
                        HEX4 <= "0100100";
                  end if;

                  if( SW( 8 downto 0 ) = "000000000" ) then --0%
                        HEX5 <= "1000000";
                        HEX4 <= "1000000";
                  end if;

                  if( SW( 8 downto 0 ) = "111111111" ) then
                        HEX7     <= "0010010"; -- S
                        HEX6     <= "0110000"; -- 3
                        HEX5     <= (others => '1');
                        HEX4     <= (others => '1');
                        HEX3     <= "0000110"; -- E
                        HEX2     <= "0101111"; -- r
                        HEX1     <= "0101111"; -- r

                  end if;
            end if;
      end if;
end process;

up_down_counter_1: process( CLOCK_50, cnt_out_int,rco_int,reg_out)
begin
      if( rco_int = '1' ) then
            cnt_out_int <= reg_out;
      elsif( rising_edge(CLOCK_50) ) then
            if( rco_int = '0' and pwm_int = '1' and cnt_out_int >
"000000000") then
                  cnt_out_int <= cnt_out_int - "000000001";
            elsif( rco_int = '0' and pwm_int = '0' and cnt_out_int <
"111110100") then
                  cnt_out_int <= cnt_out_int + "000000001";
            end if;
      end if;
end process;

counter_trans_1:  process(  cnt_out_int,  rco_int,  CLOCK_50,  enabe,
pwm2_en )
begin
      if( enabe = '0' or pwm2_en = '1' ) then
            rco_int <= '1';
      elsif( rising_edge(CLOCK_50) ) then
            if((  cnt_out_int  =  "111110100")  or  (cnt_out_int  =
"000000000")) then
                  rco_int <= '1';
            else
                  rco_int <= '0';
            end if;
```

```
      end if;
end process;

pwm_generator_1:process(  CLOCK_50,  rco_int,  enabe,  pwm2_en,  pwm_int,
fullperiod1 )
begin
      if( enabe = '0'  or pwm2_en = '1' ) then
            pwm_int <= '0';
            fullperiod1 <= 0;
      elsif( rising_edge(rco_int) ) then
            pwm_int <= NOT(pwm_int);
            fullperiod1 <= fullperiod1 + 1;
            if(fullperiod1 = 2) then
                  fullperiod1 <= 0;
            end if;
      else
            pwm_int <= pwm_int;
      end if;
end process;

up_down_counter_2:process( CLOCK_50, cnt_out_int2,rco_int2,reg_out)
begin
      if( rco_int2 = '1' ) then
            cnt_out_int2 <= reg_out;
      elsif( rising_edge(CLOCK_50) ) then
            if( rco_int2 = '0' and pwm_int2 = '1' and cnt_out_int2 >
"000000000") then
                  cnt_out_int2 <= cnt_out_int2 - "000000001";
            elsif( rco_int2 = '0' and pwm_int2 = '0' and cnt_out_int2 <
"111110100") then
                  cnt_out_int2 <= cnt_out_int2 + "000000001";

            end if;
      end if;
end process;

counter_trans_2:process(   cnt_out_int2,   rco_int2,   CLOCK_50,   enabe,
pwm2_en )
begin
      if( enabe = '0' or pwm2_en = '0' ) then
            rco_int2 <= '1';
      elsif( rising_edge(CLOCK_50) ) then
            if((   cnt_out_int2   =   "111110100")   or   (cnt_out_int2   =
"000000000")) then
                  rco_int2 <= '1';
            else
                  rco_int2 <= '0';
            end if;
      end if;
end process;

pwm_generator_2: process( CLOCK_50, rco_int2, enabe, pwm2_en, pwm_int2,
fullperiod2 )
begin
      if( enabe = '0' or pwm2_en = '0') then
            pwm_int2 <= '0';
            fullperiod2 <= 0;
```

```
      elsif( rising_edge(rco_int2) ) then
            pwm_int2 <= NOT(pwm_int2);
            fullperiod2 <= fullperiod2 + 1;
            if(fullperiod2 = 2) then
                  fullperiod2 <= 0;
            end if;
      else
            pwm_int2 <= pwm_int2;
      end if;
end process;

pwm_control_uplow: process( fullperiod1, fullperiod2, enabe  )
begin
      if( enabe = '0' ) then
            pwm4_en <= '0';
      end if;

      if(fullperiod3 = 2) then
            pwm4_en <= '1';
      end if;

      if(fullperiod4 = 2) then
            pwm4_en <= '0';
      end if;
end process;

up_down_counter_3: process( CLOCK_50, cnt_out_int3, rco_int3 )
begin
      if( rco_int3 = '1' ) then
            cnt_out_int3 <= "111000000";
      elsif( rising_edge(CLOCK_50) ) then
            if( rco_int3 = '0' and pwm_int3 = '1' and cnt_out_int3 >
"000000000") then
                  cnt_out_int3 <= cnt_out_int3 - "000000001";
            elsif( rco_int3 = '0' and pwm_int3 = '0' and cnt_out_int3 <
"111110100") then
                  cnt_out_int3 <= cnt_out_int3 + "000000001";

            end if;
      end if;
end process;

counter_trans_3:  process(  cnt_out_int3,  rco_int3,  CLOCK_50,  enabe,
pwm4_en )
begin
      if( enabe = '0' or pwm4_en = '1' ) then
            rco_int3 <= '1';
      elsif( rising_edge(CLOCK_50) ) then
            if((  cnt_out_int3  =  "111110100")  or  (cnt_out_int3  =
"000000000")) then
                  rco_int3 <= '1';
            else
                  rco_int3 <= '0';
            end if;
      end if;
end process;
```

```
pwm_generator_3:process( CLOCK_50, rco_int3, enabe, pwm4_en, pwm_int3,
fullperiod3 )
begin
      if( enabe = '0'  or pwm4_en = '1' ) then
            pwm_int3 <= '0';
            fullperiod3 <= 0;
      elsif( rising_edge(rco_int3) ) then
            pwm_int3 <= NOT(pwm_int3);
            fullperiod3 <= fullperiod3 + 1;
            if(fullperiod3 = 2) then
                  fullperiod3 <= 0;
            end if;
      else
            pwm_int3 <= pwm_int3;
      end if;
end process;

up_down_counter_4:process( CLOCK_50, cnt_out_int4, rco_int4 )
begin
      if( rco_int4 = '1' ) then
            cnt_out_int4 <= "111000000";
      elsif( rising_edge(CLOCK_50) ) then
            if( rco_int4 = '0' and pwm_int4 = '1' and cnt_out_int4 >
"000000000") then
                  cnt_out_int4 <= cnt_out_int4 - "000000001";
            elsif( rco_int4 = '0' and pwm_int4 = '0' and cnt_out_int4 <
"111110100") then
                  cnt_out_int4 <= cnt_out_int4 + "000000001";

            end if;
      end if;
end process;

counter_trans_4:process(  cnt_out_int4,  rco_int4,  CLOCK_50,  enabe,
pwm4_en )
begin
      if( enabe = '0' or pwm4_en = '0' ) then
            rco_int4 <= '1';
      elsif( rising_edge(CLOCK_50) ) then
            if((  cnt_out_int4  =  "111110100")  or  (cnt_out_int4  =
"000000000")) then
                  rco_int4 <= '1';
            else
                  rco_int4 <= '0';
            end if;
      end if;
end process;

pwm_generator_4: process( CLOCK_50, rco_int4, enabe, pwm4_en, pwm_int4,
fullperiod4 )
begin
      if( enabe = '0' or pwm4_en = '0') then
            pwm_int4 <= '0';
            fullperiod4 <= 0;
      elsif( rising_edge(rco_int4) ) then
            pwm_int4 <= NOT(pwm_int4);
            fullperiod4 <= fullperiod4 + 1;
```

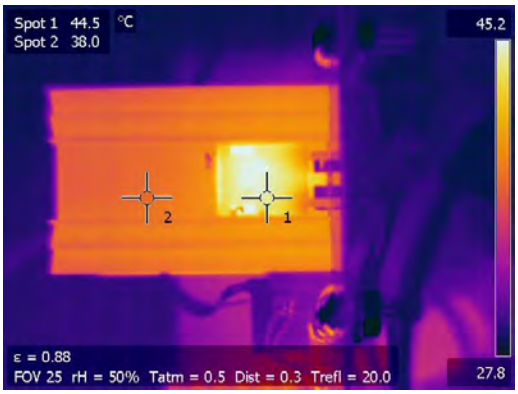
```
            if(fullperiod4 = 2) then
                  fullperiod4 <= 0;
            end if;
      else
            pwm_int4 <= pwm_int4;
      end if;
end process;


LEDR(17) <= pwm_int;
LEDR(16) <= pwm_int2;
LEDR(15) <= pwm_int3;
LEDR(14) <= pwm_int4;
GPIO_0(0) <= pwm_int;
GPIO_0(1) <= pwm_int2;
GPIO_0(2) <= pwm_int3;
GPIO_0(3) <= pwm_int4;
LEDG     <= (others => '0');
GPIO_0(4) <= '0';
GPIO_0(5) <= '0';
GPIO_0(6) <= '0';
GPIO_0(7) <= '0';
GPIO_0(8) <= '0';
GPIO_0(9) <= '0';
GPIO_0(10) <= '0';
GPIO_0(11) <= '0';
GPIO_0(12) <= '0';
GPIO_0(13) <= '0';
GPIO_0(14) <= '0';
GPIO_0(15) <= '0';
GPIO_0(16) <= '0';
GPIO_0(17) <= '0';
GPIO_0(18) <= '0';
GPIO_0(19) <= '0';
GPIO_0(20) <= '0';
GPIO_0(21) <= '0';
GPIO_0(22) <= '0';
GPIO_0(23) <= '0';
GPIO_0(24) <= '0';
GPIO_0(25) <= '0';
GPIO_0(26) <= '0';
GPIO_0(27) <= '0';
GPIO_0(28) <= '0';
GPIO_0(29) <= '0';
GPIO_0(30) <= '0';
GPIO_0(31) <= '0';
GPIO_0(32) <= '0';
GPIO_0(33) <= '0';
GPIO_0(34) <= '0';
GPIO_0(35) <= '0';



end arch_PWM;
```

Appendix B: MATLAB Transformer Design M-File

```
% Design a high-frequency transformer for a full bridge converter
Pout = 5000.0;      % converter rated output power
fs = freqsw;       % transformer frequency
fskHz = fs/1000.0;
Voutconv = 200.0;       % Converter output voltage

Vin = 400.0;        % desired input voltage
Vout = 400.0;       % desired output voltage
D = 0.5;       %Anticipated duty cycle
delIl = 2.5;     %Anticipated current ripple
Ioutmax = Pout/Voutconv;   % anticipated maximum current

N2oN1 = Vout/(Vin);    % transformer turns ratio

I2rms = sqrt(Ioutmax^2+(1/12)*(delIl)^2)*sqrt(D);
I1rms = I2rms*N2oN1;
Itot = I1rms + (N2oN1)*I2rms;

lam1 = (Vin*D)/fs;
res = 1.724e-6;      % resistivity of copper ohm-cm

% P-type ferrite material from Magnetics Inc
% for 100kHz < fs < 500kHz
% Pcore,loss = 0.0434*(fskHz^1.63)*(BkG^2.62) in mW/cm^3
beta = 2.62;
Kfe = 0.0434*(fskHz^1.63)*(10^beta)/1000
Ku = 0.2;            % reasonable fill factor for a toroid
% allowable losses (core + copper) in transformer 0.5%
Plosstot = 0.005*Pout;

fac1 = Kfe^(2/beta);
fac2 = Plosstot^((beta+2)/beta);
Kgfemin = (1e8)*res*lam1*lam1*Itot*Itot*fac1/(4*Ku*fac2);

cn = n;         % cycle through core population
WA = Wacm2(cn);
MLT = MLTcm(cn);
AC = Acm2(cn);
LM = Lcm(cn);

adequate = boolean(Kcore(n) > Kgfemin)

numdelB = (1e8)*res*lam1*lam1*Itot*Itot*MLT;
dendelB = 2*Ku*WA*AC*AC*AC*LM*beta*Kfe;
exp1 = 1.0/(beta+2);
delB = (numdelB/dendelB)^(exp1)

N1 = (1e4)*lam1/(2*delB*AC)
N2 = N2oN1*N1

Aw1max = 0.5*Ku*WA/N1
```

```
    Aw2max = 0.5*Ku*WA/N2

    % for P-type material mu_rel = 2500
    muo = 4*pi*1e-7;
    mur = 2500.0;
    Lm1 = 0.01*muo*mur*N1*N1*AC/LM
    Impk = lam1/(2*Lm1)
    R1 = res*N1*MLT/Aw1max
    R2 = res*N2*MLT/Aw2max

    % wire cross-sectional areas in cm^2
    %   AWG     cm^2
    wiresize = [26, 24, 22, 20, 18, 16, 14, 12, 10, 8, 6, 4, 2];
    barearea = 1e-3*[1.28, 2.047, 3.243, 5.188, 8.228, 13.07, 20.02,
33.08, 52.41, 83.67, 133.0, 211.5, 336.3];

    coil1gage = wiresize(max(find(barearea <= Aw1max)))
    coil2gage = wiresize(max(find(barearea <= Aw2max)))

    currdensity1 = I1rms/barearea(max(find(barearea <= Aw1max)))
    currdensity2 = I2rms/barearea(max(find(barearea <= Aw2max)))

    Pcu = res*MLT*N1*N1*Itot*Itot/(WA*Ku)
    Pcore = Kfe*(delB^beta)*AC*LM
    Ptotall = Pcu + Pcore;
```

Appendix C: Full Si IR Testing Data



Appendix Figure 18 - Si Device IR Screenshot after 5 minutes of operation; $T_{sink,f}$ = 44.5 ºC

Appendix Figure 2 - Si Device IR Screenshot after 5 minutes of operation; $T_{sink,f}$ = 50.5 ºC

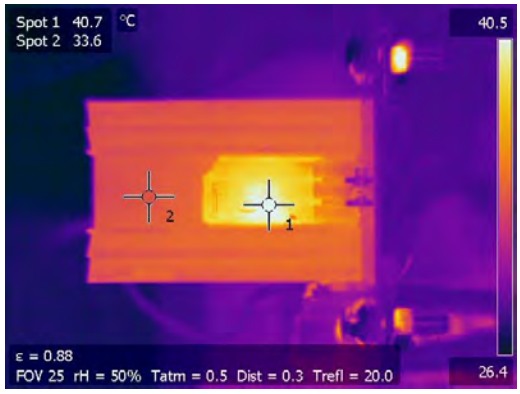
Appendix Figure 3 - Si Device IR Screenshot after 5 minutes of operation; $T_{sink,f}$ = 58.1 ºC

Appendix Figure 4 - Si Device IR Screenshot after 5 minutes of operation; $T_{sink,f}$ = 64.2 ºC

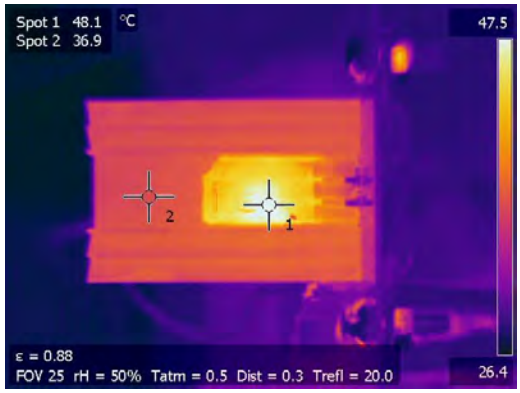
Appendix Figure 5 - Si Device IR Screenshot after 5 minutes of operation; $T_{sink,f}$ = 65.5 ºC

Appendix Figure 6 - Si Device IR Screenshot after 5 minutes of operation; $T_{sink,f}$ = 70.9 ºC

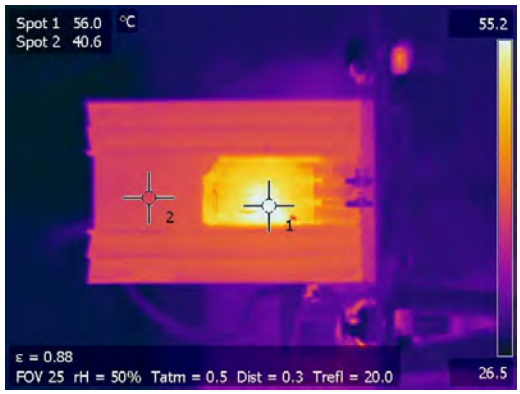
Appendix D: Full SiC IR Testing Data Set



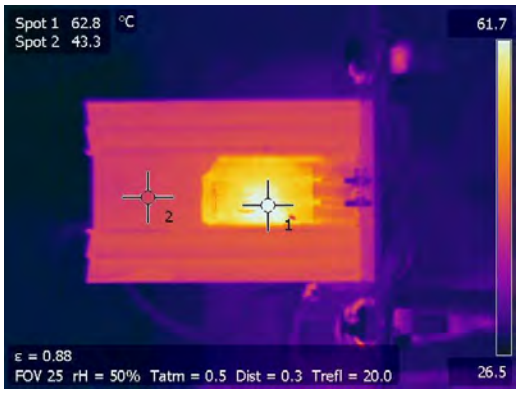
Appendix Figure 7 - SiC Device IR Screenshot at maximum throughput power; Tj,f = 40.7 ºC



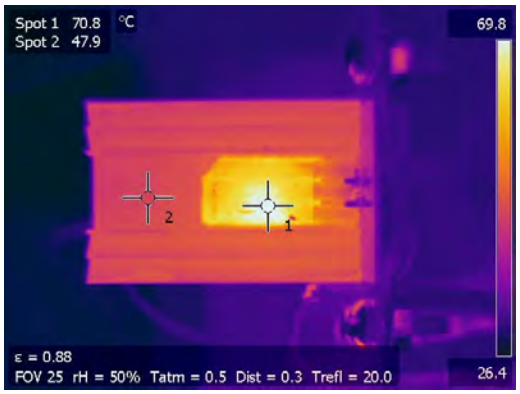
Appendix Figure 8 - SiC Device IR Screenshot at maximum throughput power; Tj,f = 48.1 ºC



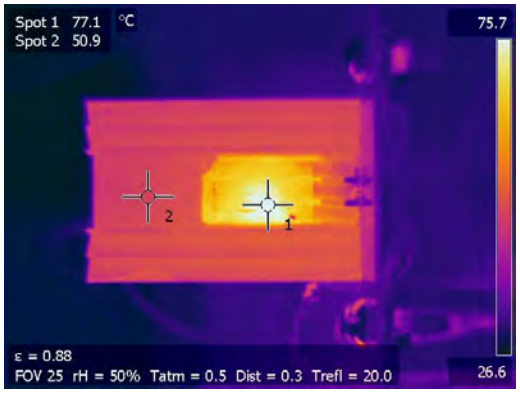
Appendix Figure 9 - SiC Device IR Screenshot at maximum throughput power; Tj,f = 56.0 ºC



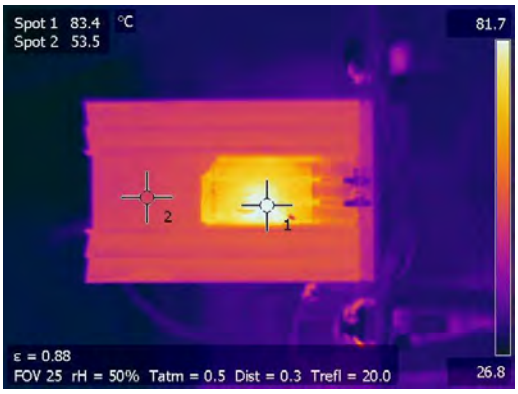
Appendix Figure 10 - SiC Device IR Screenshot at maximum throughput power; Tj,f = 62.8 ºC



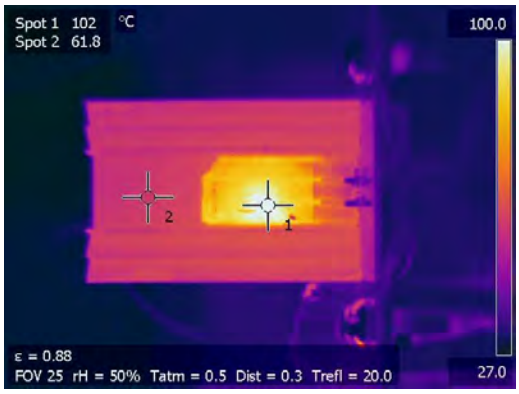
Appendix Figure 11 - SiC Device IR Screenshot at maximum throughput power; Tj,f = 70.8 ºC



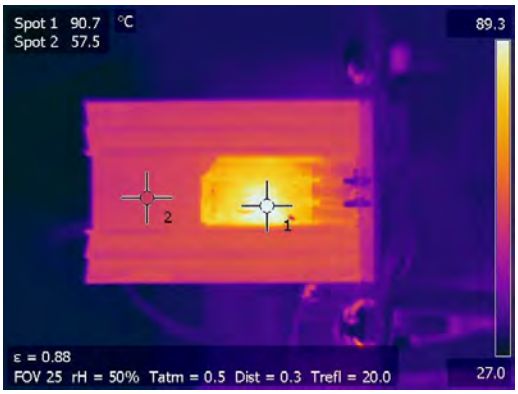
Appendix Figure 12 - SiC Device IR Screenshot at maximum throughput power; Tj,f = 77.1 ºC



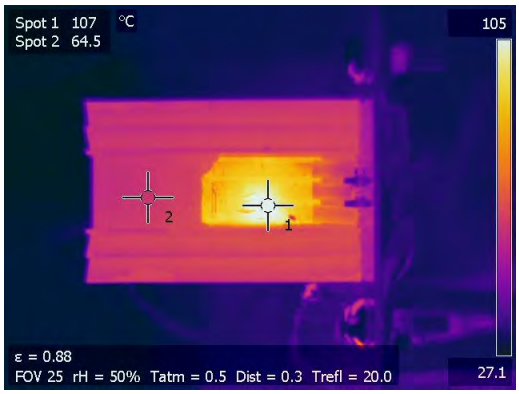
Appendix Figure 13 - SiC Device IR Screenshot at maximum throughput power; Tj,f = 83.4 ºC



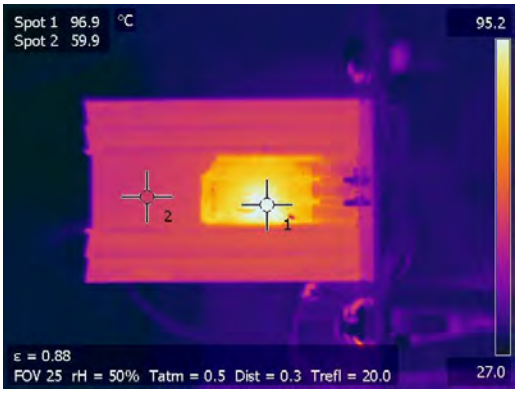
Appendix Figure 17 - SiC Device IR Screenshot at maximum throughput power; Tj,f = 101.8 ºC



Appendix Figure 14 - SiC Device IR Screenshot at maximum throughput power; Tj,f = 90.7 ºC



Appendix Figure 18 - SiC Device IR Screenshot at maximum throughput power; Tj,f = 107 ºC



Appendix Figure 16 - SiC Device IR Screenshot at maximum throughput power; Tj,f = 96.9 ºC